BlueX Microelectronics Co., Ltd.

Bluetooth 5.0 **LE | MESH** SoC

Datasheet of RF03

(with 4Mb Flash)

DS-RF03-01

Version 3.2

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http://www.bluexmicro.com

Table of Contents

1 General description

The RF03 is a System-on-Chip combining an application processor, memories, cryptography engine, power management unit, digital and analog peripherals and a MAC engine complied with Bluetooth® Low Energy 5.0 and radio transceiver.

A 32-bit MCU is integrated in RF03 for BLE link layer management and system operation. Rich digital and analog peripheral interfaces are optimized for external control, including GPIO, UART, IIC, PWM and LDOs. Power Management Unit with on-chip DCDC buck converter and various Regulators provides ultra-low current consumption for RF03.

2 Feature list

- **Complies with Bluetooth 5.0 with 1M / 2M bps data rates.**

- **Radio Transceiver**
  - -93 dBm RX sensitivity at 1Mbps mode
  - -90 dBm RX sensitivity at 2Mbps mode
  - RF output power levels: -20dBm, 0dBm, 3dBm and 8dBm
  - 50dB RSSI dynamic range

- **Supply Current**
  - 4.3mA in RX and 4.4mA in TX with On Chip DCDC Converter@4.3V
  - 5.5mA in RX and 5.7mA in TX with On Chip DCDC Converter@3.3V

- **Ultralow Current Mode**
  - Sleep current : 2.5uA ~ 6uA，SRAM (16 KB ~ 208 KB) retention
  - Average current: 20uA，during 1.28 sec cycle time (Active / Sleep)
    Notice: Active (Broadcasting ADV) / Sleep (208 KB SRAM retention)

- **Analog Interfaces**
  - 1 Embedding ADC in pin VBAT with Battery monitoring function from 5.5V to 2.0V
  - Temperature sensor from -40℃ to 125℃

- **Digital Interfaces**
  - Up to 10 GPIOs
  - 1 Internal Quad-SPI Flash interface
  - 2 UART - Flow control up to 1Mbps and supports all the baud rate under 1Mbps, IRDA is supported
  - 2 IIC - Master / Slave programmable and speed up to 1Mbps
  - 2 Timers and 1 Watch-dog Timer
  - 5 PWM Outputs

- **Integrated 32-bit MCU**
  - Clock frequency: 16MHz, 32MHz (Major) , 48MHz, 64MHz, 80MHz and 96MHz (Max)
  - CPU Benchmarking : 2.07 Coremark / MHz
  - SWD debug interface
  - AHB / APB bus matrix with speed up to 96MHz

- **Memories**
  - 128 KB ROM (Boot ROM and BLE stack)
  - 512 KB Flash
  - 208 KB SRAM
    - Composed of 6 pages of 32KB and 1 page of 16KB , with retention capability
    - Each 32KB can be set into retention state separately and exchange memory for BLE connection data
    - 16KB of 4 way cache controller for external SPI flash which enable CPU run on the external SPI flash, this 16KB cache can be also used as system SRAM when cache is disabled

Power Management

- 2.3-5.0V power input
- One 1.2V Integrated DCDC buck converter
- One 1.8V LDO with 40mA output
- Two 3.3V LDO with 50mA & 25mA output each

Cryptographic Engine

- ECC
- AES-128

Package

- QFN32 (4 X 4 mm^2)

Operating Temperature

- -25℃ to 85℃

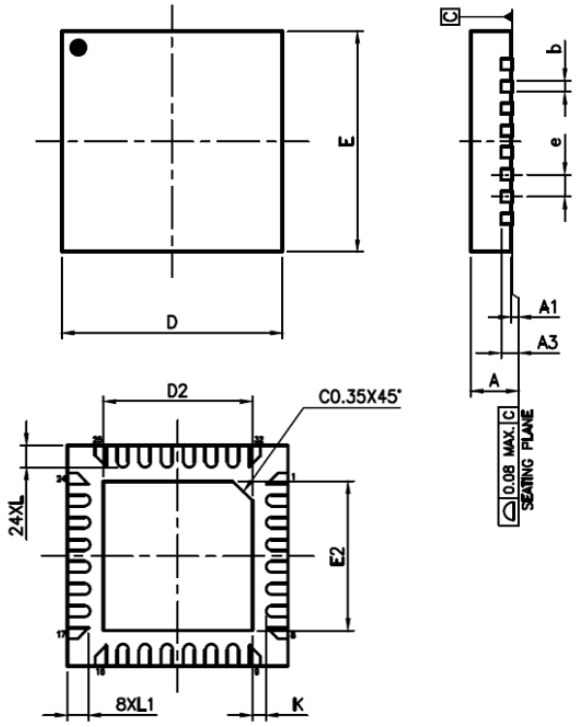
3 Package

3.1 RF03-- QFN 32 pins Package (4 mm x 4 mm) with 4Mb Flash

Pin	Symbol	Type	Description
1	P02	DIO	FUNC_IO02/GPIO02
2	P15	DIO	FUNC_IO13/GPIO15
3	P16	DIO	FUNC_IO14/GPIO16
4	P17	DIO	FUNC_IO15/GPIO17
5	P12	DIO	FUNC_IO10/GPIO12
6	P13	DIO	FUNC_IO11/GPIO13
7	VDD_3V_1	PO	Supply to external 3.3V
8	VDD_1V8	PO	Supply to external 1.8V
9	VDD_DIG	PI	Digital circuit power supply
10	VDD_1V2	PO	DC/DC Converter output
11	VDD_BAT	PI	Battery supply voltage
12	Ext Reset	DI	Pull low internally. High active.
13	P00	DIO	SWCLK/GPIO00
14	P01	DIO	SWDIO/GPIO01
15	VDD_CPU	PO	VDD_CPU output
16	VDD_AWO	PO	VDD_AWO output
17	P22	DIO	FUNC_IO20/GPIO22

Pin	Symbol	Type	Description
18	P23	DIO	FUNC_IO21/GPIO23
19	XTAL32K_P	AI	32.768 kHz Crystal input (+)
20	XTAL32K_N	AI	32.768 kHz Crystal input (-)
21	VDD_3V_2	PO	Supply to external 3.3V
22	VDD_BAT_2	PI	Guard ring power supply
23	VDD_VCO	PI	VCO power supply
24	LOOP_C	AIO	PLL loop filter external capacitor.
25	VDD_CP	PI	PLL power supply
26	VDD_RF1	PI	RF power supply
27	RF_P	AIO	RF input/output
28	RF_N	AIO	RF input/output
29	VDD_A	PI	Power supply for an analog circuit
30	VDD_BAT_1	PI	ADC power supply
31	XTAL32M_P	AI	32 MHz Crystal input (+)
32	XTAL32M_N	AI	32 MHz Crystal input (-)
IC Ground pad		GND	Backside GND plane. Must be connected to the GND.

NOTE: AI : analog input AO : analog output AIO : analog input/output DI : digital input DIO : digital input/output PI : power input PO : power output



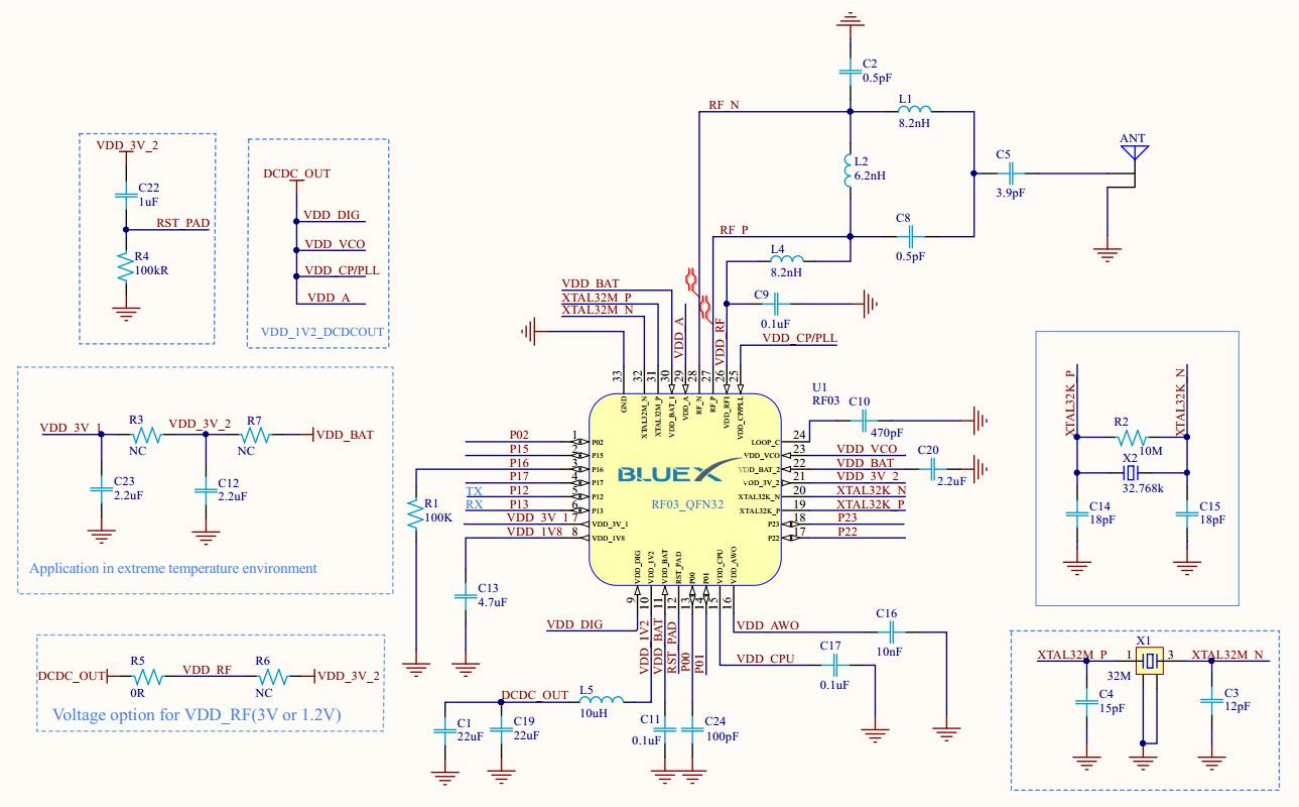
PKG CODE	VQFN			
SYMBOLS	MIN.	NOM.	MAX.	UNIT
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	
A3	0.203 REF			
b	0.15	0.20	0.25	
D	4.00 BSC			
E	4.00 BSC			
e	0.40 BSC			
K	0.20	-	-	
Lead Frame PAD SIZE	114 X 11* MIL			
SYMBOLS	MIN.	NOM.	MAX.	UNIT
D2	2.65	2.70	2.75	mm
E2	2.65	2.70	2.75	
L	0.35	0.40	0.45	

3.2 IR Reflow Temperature-Time Profile

	Ave Ramp up rate(T)	Holding Time	Peak Temp.	Liquidus Temp.	Time Above Temp.	Ave Cooling rate(T)	Result
Boundary	217.00-260.00 C	150.00-200.00 C	--------	217.00 C	255.00 C	260.00-217.00 C	
Range	0.00-3.00 (C/sec)	60.00-120.00 (sec)	260.00-265.00 (C)	60.00-150.00 (sec)	30.00-40.00 (sec)	6.00-0.00 (C/sec)	
sensor1	0.63	90.00	260.90	101.00	30.00	1.87	OK

3.3 Application circuit

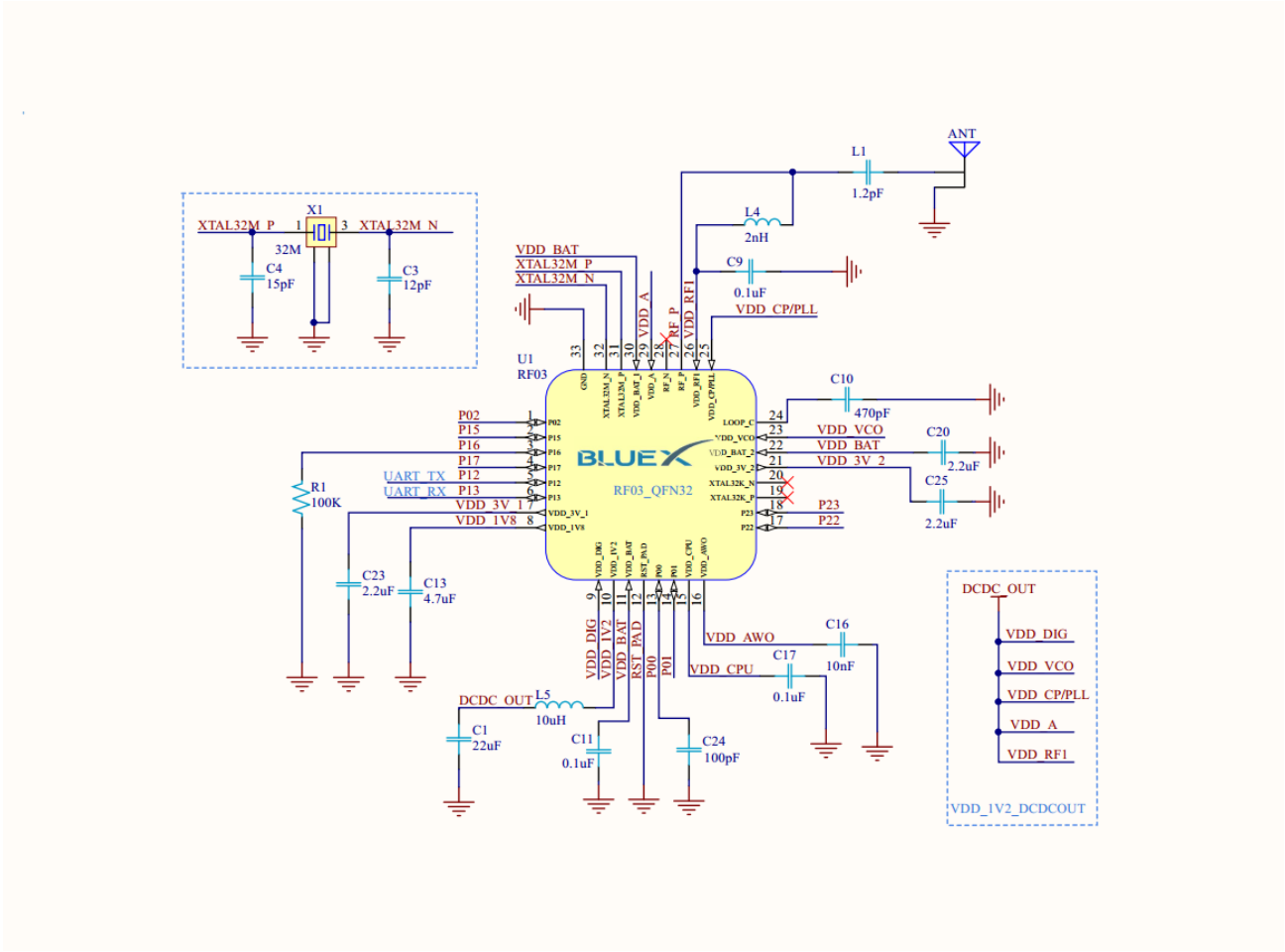
3.3.1 General application circuit



■ Circuit Features

Component	TX PWR.	RX SEN.	LXT	RF CKT. Structure
Standard: 30 PCS Option : Add 2 PCS	+8 dBm(Max.)	1Mbps: -93 dBm 2Mbps: -90 dBm	Option	Differential

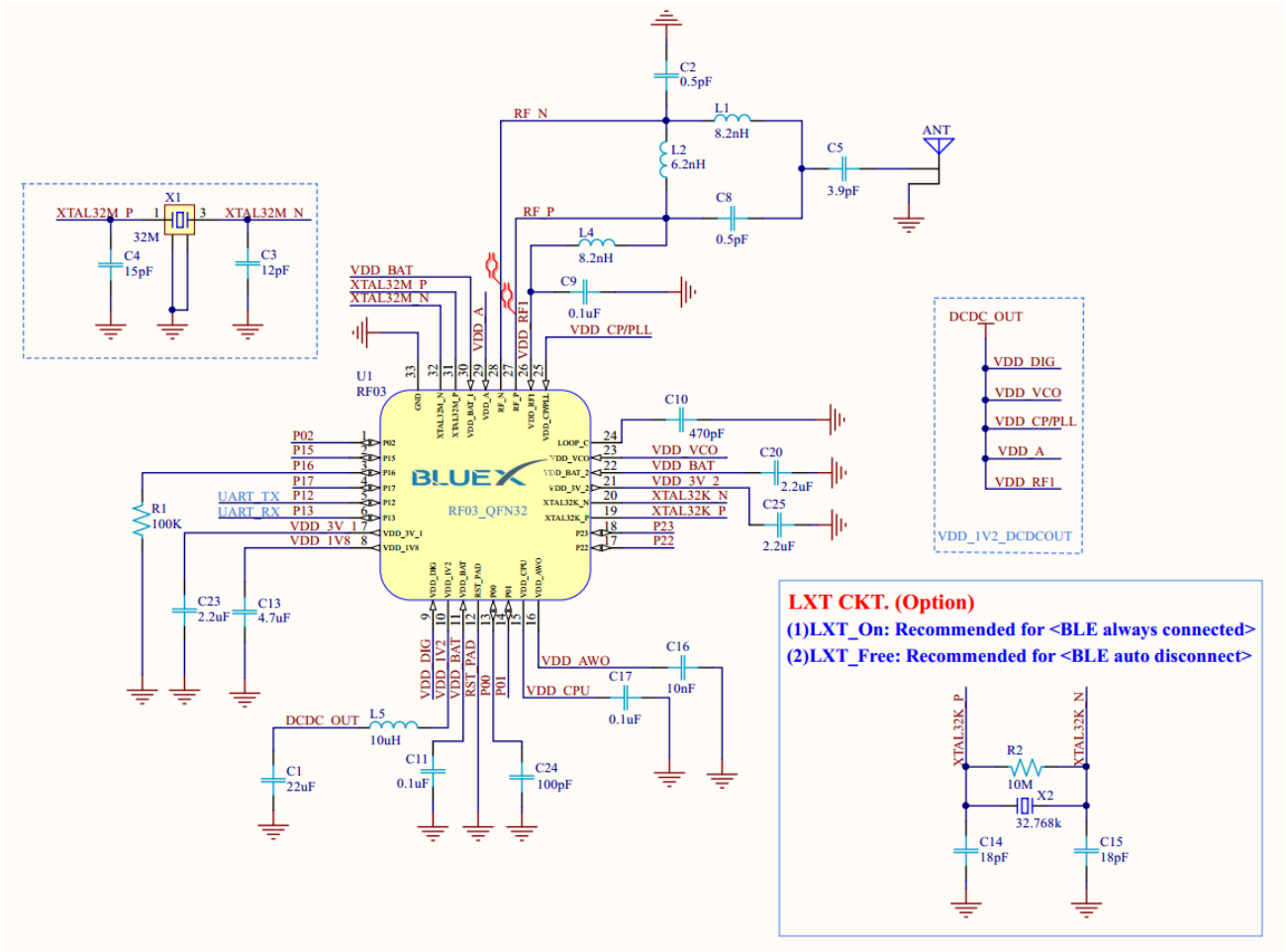
3.3.2 Single-End with DC/DC Bucker available, TX PWR: -3dBm (Max)



■ Circuit Features

Component	TX PWR.	RX SEN.	LXT	RF CKT. Structure
18 PCS	-2 dBm(Max.)	1Mbps: -90 dBm 2Mbps: -86 dBm	LXT - free	Single-End

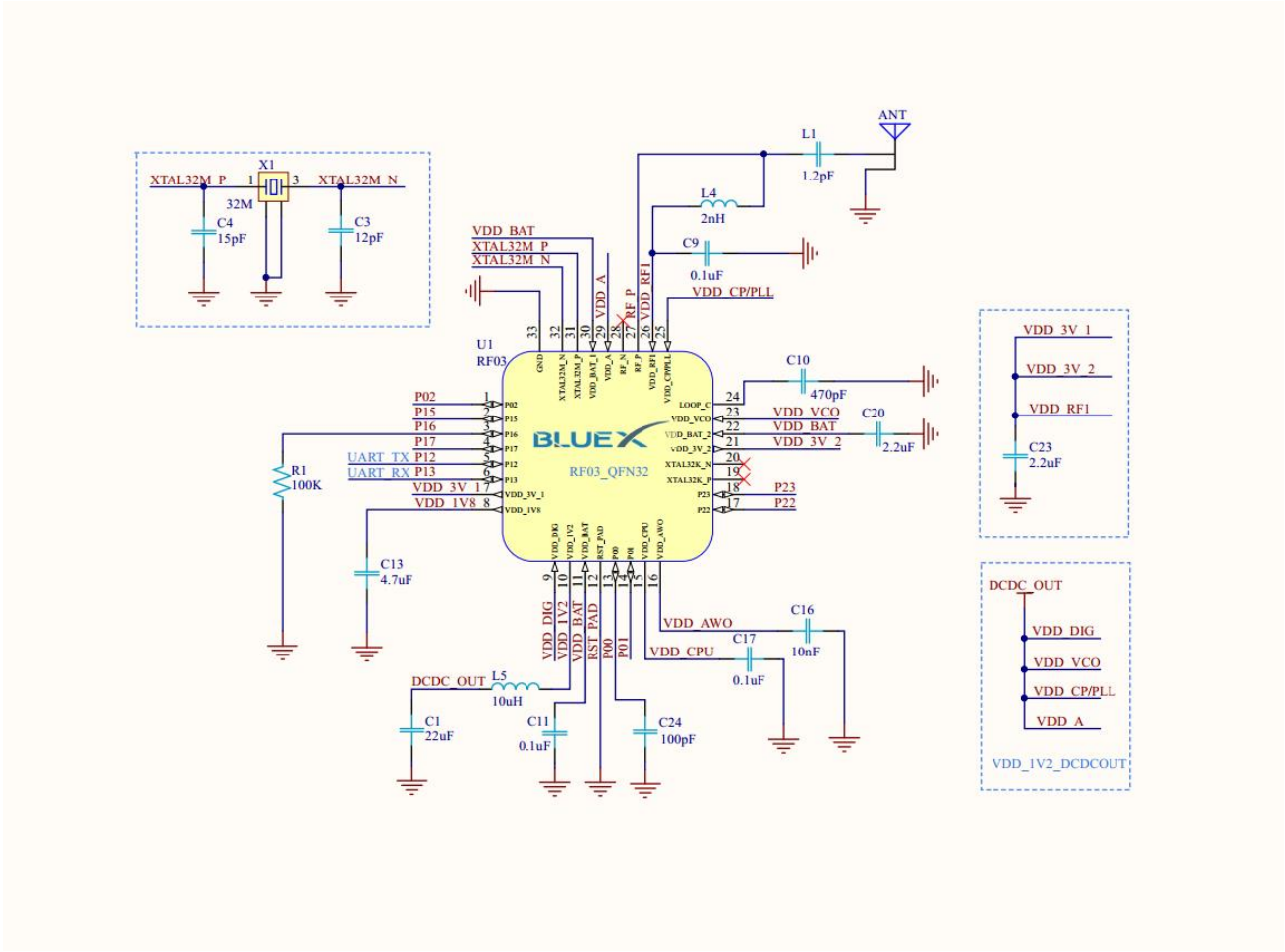
3.3.3 Differential with DC/DC Bucker available, TX PWR: +2dBm(Max)



■ Circuit Features

Component	TX PWR.	RX SEN.	LXT	RF CKT. Structure
Standard: 26 PCS Option : Reduce 4 PCS	+2 dBm(Max.)	1Mbps: -93 dBm 2Mbps: -90 dBm	Option	Differential

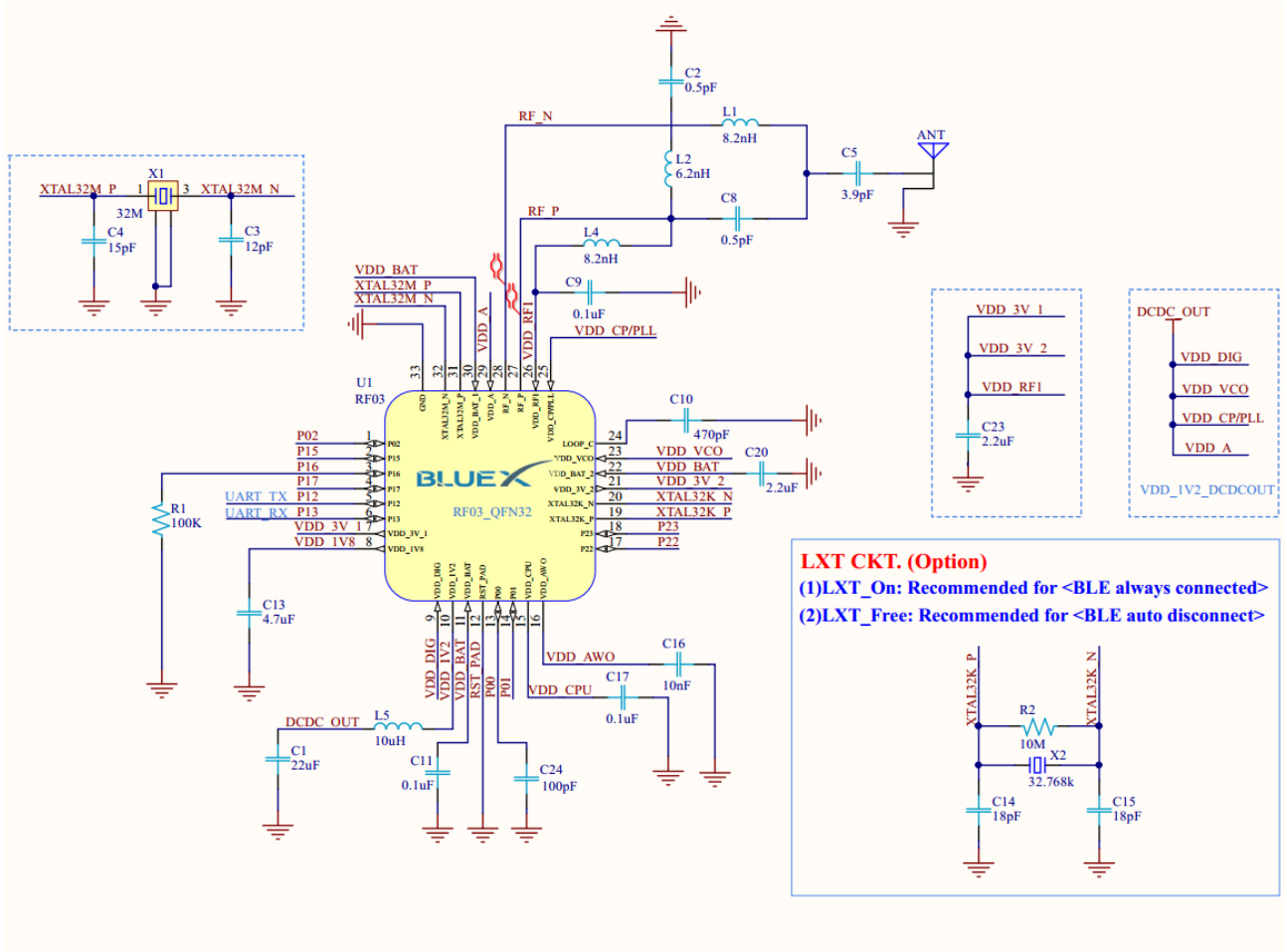
3.3.4 Single-End with DC/DC Bucker available, TX PWR: +4dBm(Max)



■ Circuit Features

Component	TX PWR.	RX SEN.	LXT	RF CKT. Structure
17 PCS	+4 dBm(Max.)	1Mbps: -90 dBm 2Mbps: -86 dBm	LXT - free	Single-End

3.3.5 Differential with DC/DC Bucker available, TX PWR: +8dBm(Max)



■ Circuit Features

Component	TX PWR.	RX SEN.	LXT	RF CKT. Structure
Standard: 22 PCS Option : Reduce 4PCS	+8 dBm(Max.)	1Mbps: -93 dBm 2Mbps: -90 dBm	Option	Differential

4 System overview

4.1 Electronical Characteristics

4.1.1 Absolute maximum ratings

Parameters	Min	Max	Unit
Storage temperature	-40	+120	°C
Voltage applied to inputs	-0.5	+5.5	V

4.1.2 Recommended Operating Conditions

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	-25		+85	℃
Supply Voltage for VDD_BAT	2.3	4.3	5.0	V
Logical high input voltage (for DI type pins)	0.85 x VDD_IO (*)		VDD_IO	V
Logical low input voltage (for DI type pins)	0		0.2 x VDD_IO	V

Note : VDD_IO is programmable as 3.3V or 1.8V individually.

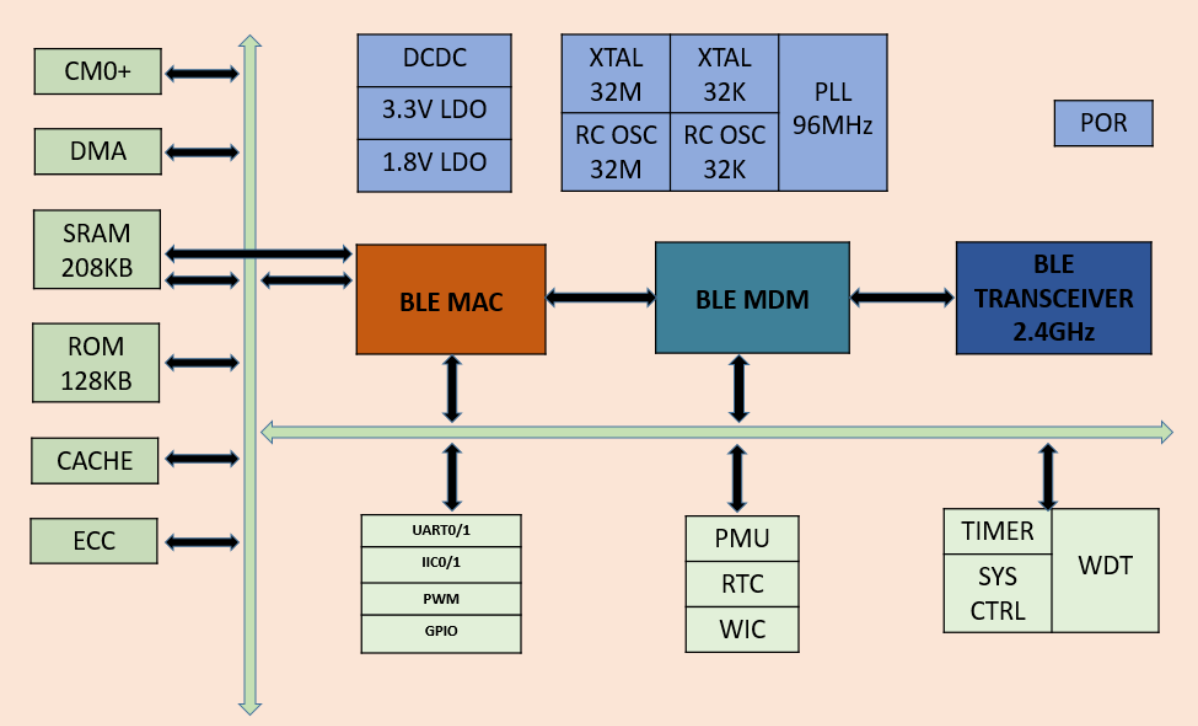
4.1.3 Radio Frequency Characteristics

TA = 25℃, VDD = 4.3 V, Frequency=2.440 GHz

Parameter	Condition	Min	Typ	Max	Unit
Receiver Sensitivity	At 1 Mbps RX Mode, 37 Byte payload length, BER<0.1%.	-93			dBm
	At 2 Mbps RX Mode, 37 Byte payload length, BER<0.1%	-90			dBm
Transmitter Output Power	Maximum RF Output Power at 0 dBm setting (Comply with Power Class 3 in Bluetooth Low Energy 5.0)	-4	-2	0	dBm
	Maximum RF Output Power at 8 dBm setting (Comply with Power Class 1.5 in Bluetooth Low Energy 5.0)	5	6.5	8	dBm
Current Consumption	Receiver with integrated DC/DC Converter		4.3		mA
	0 dBm Transmitter with integrated DC/DC Converter		4.4		mA
	8 dBm Transmitter with integrated DC/DC Converter		26		mA
	Sleep with SRAM (16KB ~ 208KB) retention, 32.768KHz Crystal Clock	2.5		6	uA
	Average current during 1.28 sec active (brofasting ADV) /sleep (SRAM 208 KB retention) cycle time		18		uA
	CPU Standby with 16MHz Clock running		1.5		mA

4.2 Block diagram

The block diagram of RF03 is shown below.



4.3 System blocks

CPU: The processor is an entry-level 32-bit processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture that is easy to learn and program.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Deterministic, high-performance interrupt handling.
- Platform security robustness, with integrated Memory Protection Unit (MPU).

BLE 5.0 MAC and PHY: This is the BLE MAC and PHY which is compatible with the BLE 5.0 protocol.

BLE RF module: This is the low power RF module which is compatible with the BLE 5.0 protocol.

Cache Controller: This is the 32bit 4 way read only cache controller which makes the CPU can run on the external flash with quard-SPI interface. The cache controller offers one cycle latency read access when the read from the CPU hit the cache. If cache miss, the cache controller is responsible to generate the SPI access command and fetch data from the external flash through quard-SPI interface.

AHB/APB bus matrix: This is the bus matrix which provides the data access channel between multiple AHB masters and multiple AHB/APB slaves. The access of different master slave pair does not affect each other which improve the data throughput of the system.

RAM controller: This is the SRAM controller which converts the AHB bus access to the 208KB SRAM read/write command. Because one of the SRAM is shared with the exchange memory used by the BLE MAC, the SRAM controller is also responsible for the arbitration between the AHB bus and the BLE MAC.

ROM controller: This is the ROM controller which converts the AHB bus access to the 128KB ROM read command. The boot code and the BLE link layer stack are stored in the ROM.

ROM patch controller: This is the data patch controller for ROM data. It provides data patching for up to 16 ROM addresses.

System controller(CPU): This is the system controller which controls the clock generator, reset generator and the pin share logic of the system. It is also responsible for frequency calibration of the 32KHz clock from RC oscillator.

DMA controller: This is the DMA controller which provides directly data access channel between the SRAM and peripheral interfaces. There are 6 DMA channels implemented in the DMA controller.

ECC engine: This is the ECC codec for the encrypt transmission of BLE. It provides hardware fast ECC calculation which costs less than 50ms for single ECC calculation.

Pin share controller: This is the pin share logic which provides flexible pin share scheme for different customers. The pin share logic is controlled by the system controller(CPU).

Clock generator(CPU): This is the clock generator which provides clock for all of the modules in the CPU power domain. It implements the clock divider, clock mux/switch and architecture clock gating for the CPU power domain.

Reset generator(CPU): This is the reset generator which provides the reset for all of the modules in the CPU power domain. It implements the reset synchronizer and the software reset logic for the CPU power domain.

UART2AHB: This is the UART interface module which provides the access channel to all of the system address space for the external UART controller. It can provide the access channel without the help of the CPU which means that even if the CPU does not work correctly, the external UART controller can access all the registers and memory space. It is mainly for debug.

Timer: This is the timer counter which is counting in a frequency programmable clock. There are two independent timer counters implemented.

Watch dog: This is the watch dog controller for the system, which can work in two modes: system reset mode and interrupt followed by system reset mode. The watch dog can prevent system from

entering some dead status by interrupt and reset the system if the system does not kick the watch dog for a long time.

System controller(PER): This is the system controller which controls the clock generator, reset generator of the PER power domain.

Clock generator(PER): This is the clock generator which provides the clock for all of the modules in the PER power domain. It implements the clock divider, clock mux/switch and architecture clock gating for the PER power domain.

Reset generator(PER): This is the reset generator which provides the reset for all of the modules in the PER power domain. It implements the reset synchronizer and the software reset logic for the PER power domain.

UART interface controller(UART0/UART1): Asynchronous serial interface controller with throughput up to 2Mbps. UART0 supports flow control and UART1 does not. Both of the UART interface controller support DMA access by DMA controller.

IIC interface controller(IIC0/IIC1): This is the IIC interface controller which can be programmed to be master or slave. It supports DMA access by DMA controller.

PWM controller: This is the PWM waveform generator which generates 5 independent PWM output signal. The frequency and the duty cycle of the PWM signal are programmable.

GPIO controller: This is the general purpose IO controller which implements 30 GPIOs. The direction and output value are both programmable. And also the interrupt mode is programmable to edge and level.

Power management unit(PMU): This is the power management controller of the system which controls the power up and power down flow for each power domain. All of the DCDC/ /LDO are controlled by PMU according to the internal FSM of the PMU.

Wakeup interrupt controller(WIC): The wakeup interrupt controller monitor the wakeup interrupts and inform the PMU to power up the system if necessary. The wakeup controller also wakeup CPU after the system has been powered up.

Mode controller: The mode controller monitor the boot select IO value during the system power up reset active period and inform the CPU from which interface the CPU can get the boot loader and the IO voltage.

Pad ring: All the digital IO cell is implemented in this module.

Power PWM controller: This controller is used to control the power output. The power output can be set to on or off. And also the power output can be set to on for some time and off for some time just like a PWM waveform.

Real time controller: This is the real time timer for the system.

System controller(AWO): This is the system controller which controls the clock generator, reset generator, power PWM, PMU, pad ring of the AWO power domain. The IO retention function is also implemented in this module.

Clock generator(AWO): This is the clock generator which provides all the clock for the AWO power domain and all the other power domain. It implements the clock divider, clock mux/switch and architecture clock gating for the AWO power domain.

Reset generator(AWO): This is the reset generator which provides all the reset for the AWO power domain and all the other power domain. It implements the reset synchronizer and the software reset logic for the AWO power domain.

4.4 Function mode

RF03 has two functional modes of operation: Mirrored mode and Cached mode.

In Mirrored mode, the system code is mirrored from the external device to the system SRAM, and CPU is running on the system SRAM. In this mode cache controller is disabled. And the 16KB SRAM used by the cache controller can be used as the normal system SRAM.

In Cached mode, the system code is stored in the external flash, and CPU is running on the external flash. In this mode cache controller is enabled and the 16KB SRAM used by the cache controller can not be used as the normal system SRAM.

Cache mode is used only when the system SRAM is not big enough for system running. Cache mode will cost more power than the mirrored mode and the performance of the CPU in cache mode is much worse than it is in the mirrored mode.

4.5 System boot sequence

After power up, power up reset will hold low for some time. Then after the power up reset is released, CPU will start to execute code from address 0x0. No address remapping is implemented in RF03 and ROM is always addressed at address 0x0. So after power up the boot sequence in the ROM is executed by CPU.

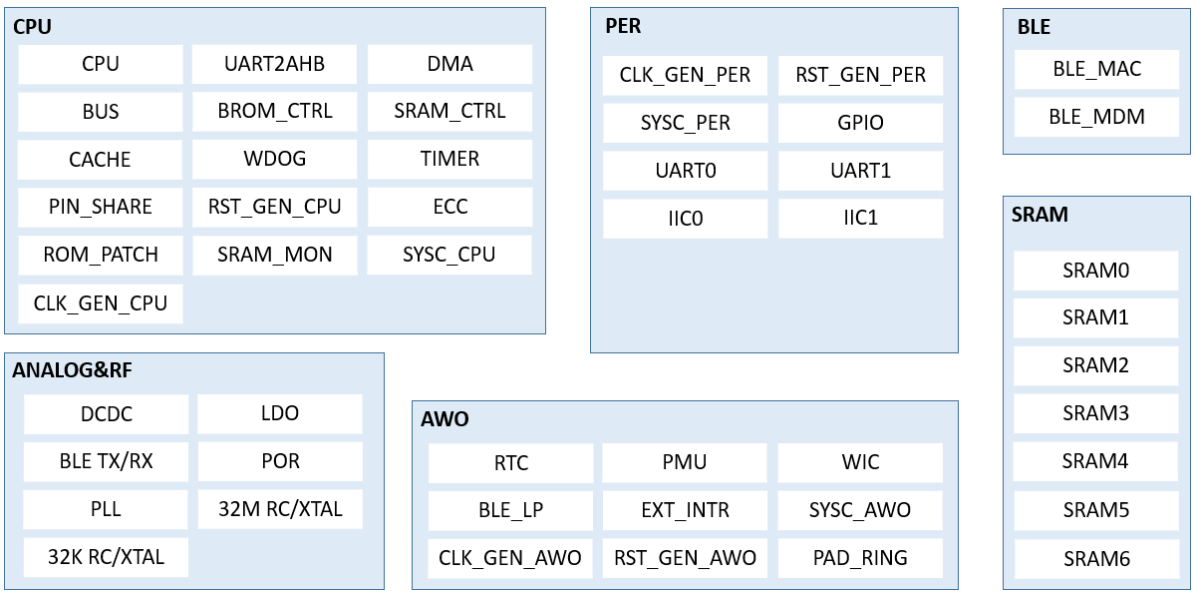
By default, all of the power sources are powered up after power on reset, and the 32MHz crystal and 32KHz RC oscillator are active. PLL is off by default. 32MHz clock is the main clock source of the system. CPU is working on 32MHz by default.

RF03 can boot from flash interface or UART interface. The IO voltage of the boot interface can be 1.8V or 3.3V. This is decided by two boot select pins. The two boot select pin shall be pulled up or pulled down to predefined value during power on reset period. The value of the boot select pins are latched to the internal boot registers during the power on reset period and be read by the CPU at the beginning of the boot sequence. Then CPU can decide which interface shall boot from and how much is the IO voltage level of the interface by reading the boot registers implemented in the system controller. The clock frequency of flash interface during boot period is 8MHz and the data rate of the UART interface during boot period is 115200bps. If boot from UART then P12 is used as TX data of UART interface and P13 is used as the RX data of UART interface.

The decode logic of the boot select pin is shown below:
P16 is pulled down means boot from flash, P16 is pulled up means boot from UART0(P12/P13). P23 is pulled down means IO voltage is 1.8V, P23 is pulled up means IO voltage is 3.3V. The default IO voltage is 1.8V.

4.6 Power domain

The block diagram of the power domain of RF03 is shown below:



RF03 is composed of 6 power domains which are CPU, PER, BLE, AWO, SRAM and ANALOG.

ANALOG power domain includes all of the analog and RF submodules and each analog and RF submodule is a dedicated sub power domain and can be powered on/off separately.

The SRAM power domain includes all of the 208kB system SRAM and is divided into 7 SRAM blocks. The size of each SRAM block is 32kB except the last block which is 16kB. Each of the 7 SRAM blocks is a dedicated sub power domain and can be powered on/off separately. The address mapping for the 7 SRAM blocks is shown below:

	start address	end address
SRAM0	0x100000	0x107FFF
SRAM1	0x108000	0x10FFFF
SRAM2	0x110000	0x107FFF
SRAM3	0x118000	0x11FFFF
SRAM4	0x120000	0x127FFF
SRAM5	0x128000	0x12FFFF
SRAM6	0x130000	0x133FFF

The PER power domain includes all of the digital peripheral interface modules. The PER power domain can work under 0.9V or 1.1V. The PER power domain can be powered off.

The BLE power domain includes BLE MAC and BLE PHY. The BLE power domain can work under 0.9V or 1.1V. The BLE power domain can be powered off.

The CPU power domain includes the core system which includes CPU, DMA, SRAM controller, bus matrix, cache controller, ECC module, system timer and system watch dog. CPU power domain can work under 0.9V or 1.1V. The CPU power domain can be powered off.

The AWO power domain includes the power management module, the IO ring, and the logic which can wake up system from sleep status which includes RTC, BLE low power counter, external interrupt controller. The AWO power domain can not be powered off. AWO power can only work under 0.9V.

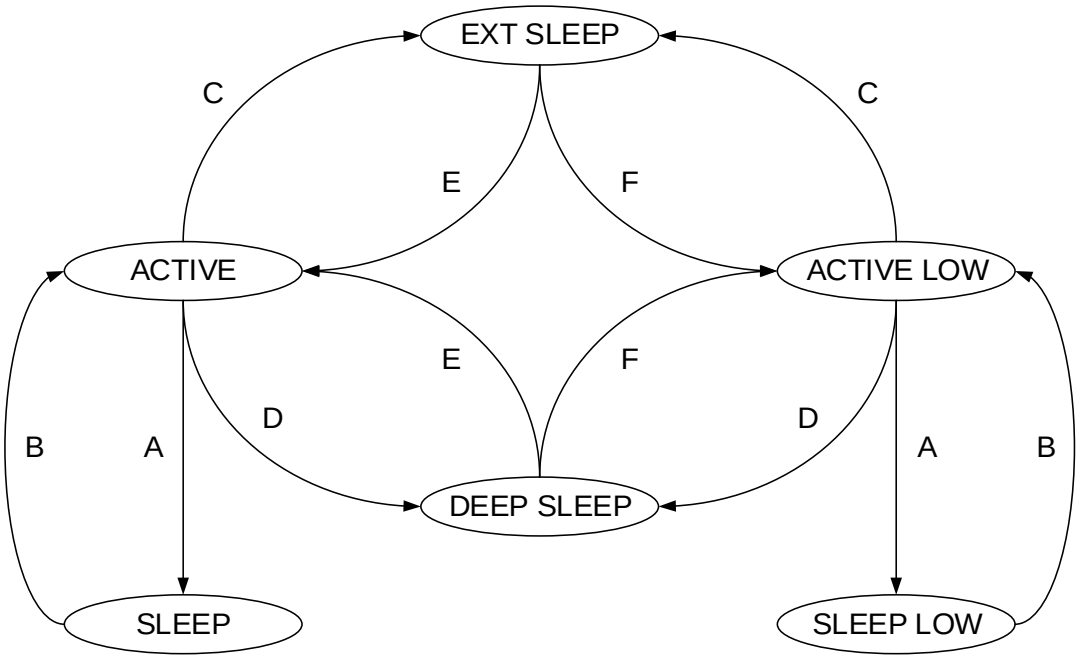
All of the other power domains except the AWO and ANALOG power domain work under the same voltage in active mode. Under inactive mode (retention mode) the voltage of SRAM can be programmed to be less than 0.9V to save leakage power of SRAM. Each of the BLE/PER/SRAM* power domains can be powered off independently. And if CPU is powered off, BLE and PER must be powered off and SRAM* must be powered off or be set to retention status. The power on and power off sequence is controlled by hardware FSM and triggered by software.

RF03 has 6 power modes which are described in the table below:

power mode	description	AWO	CPU	PER	BLE	SRAM	ANALOG
ACTIVE	AWO is working CPU is working. The working frequency of CPU is more than 32MHz, and CPU is working under 1.1V at least one of the SRAM is working(power on) all of the other power domain is on/off programmable by CPU	ON	ON	P	P	P	P
ACTIVE LOW	AWO is working CPU is working. The working frequency of CPU is equal to or less than 32MHz, and CPU is working under 0.9V at least one of the SRAM is working(power on) all of the other power domain is on/off programmable by CPU	ON	ON	P	P	P	P
SLEEP	AWO is working CPU is clock gated and the working voltage of CPU is 1.1V at least one of the SRAM is working(power on) all the other power domain is on/off programmable by CPU	ON	ON	P	P	P	P
SLEEP LOW	AWO is working CPU is clock gated and the working voltage of CPU is 0.9V at least one of the SRAM is working(power on) all the other power domain is on/off programmable by CPU	ON	ON	P	P	P	P
EXTENDED SLEEP	AWO is working under 32KHz CPU, PER and BLE are powered off At least one of the SRAM is in retention state All of the other power domain is power off	ON	OFF	OFF	OFF	ON/OFF	OFF

power mode	description	AWO	CPU	PER	BLE	SRAM	ANALOG
DEEP SLEEP	PD_AWO is working under 32KHz CPU, PER and BLE are powered off All of the SRAM are off All of the other power domain is power off	ON	OFF	OFF	OFF	OFF	OFF
Note: ON: power on OFF: power off P: ON/OFF programmable							

The power state machine of the power states is shown in the block diagram below:



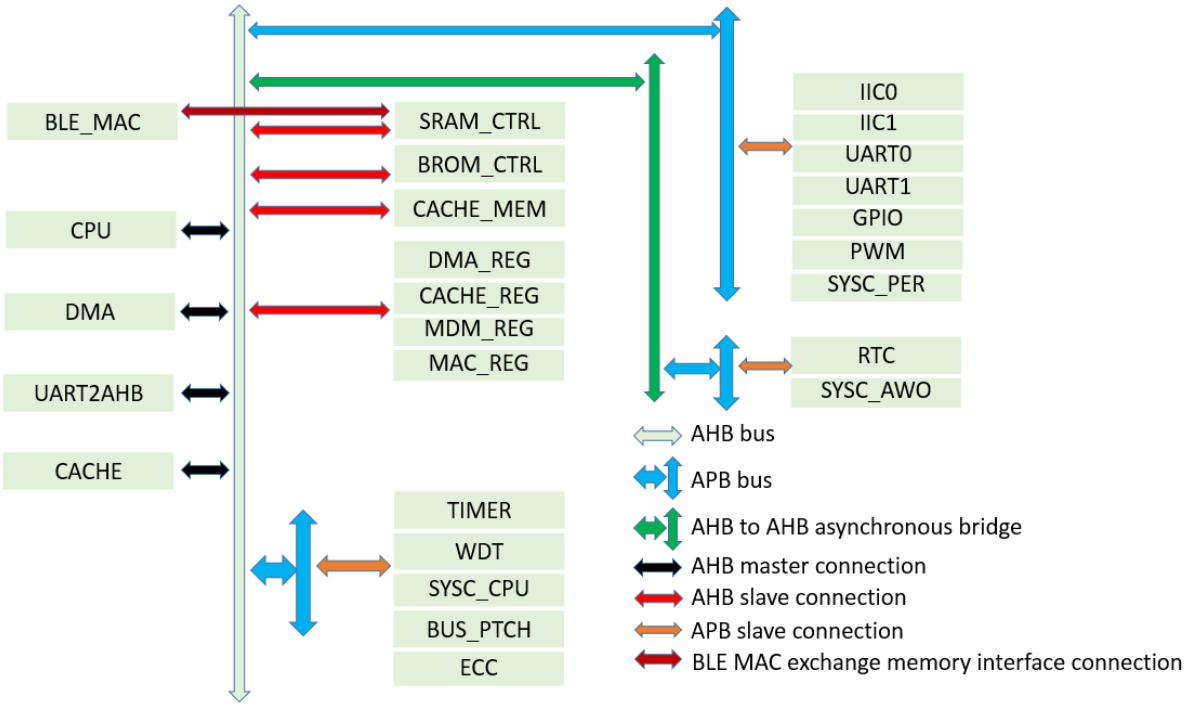
The power state transfer condition in the above diagram is shown in the table below:

A	CPU execute WFI with DEEP_SLEEP bit set to low
B	any non-masked interrupt is active
C	CPU execute WFI with DEEP_SLEEP bit set to high, and not all of the active SRAM is powered off together with CPU
D	CPU execute WFI with DEEP_SLEEP bit set to high, and all of the active SRAM are powered off together with CPU
E	Any of the external interrupt, BLE low power interrupt, RTC interrupt is active and CPU is waked up with the register VDD_VOLTAGE is set to low which means CPU will work under 1.1V after wake up
F	Any of the external interrupt, BLE low power interrupt, RTC interrupt is active and CPU is waked up with the register VDD_VOLTAGE is set to

	high which means CPU will work under 0.9V after wake up
note: register VDD_VOLTAGE is a programmable register in AWO power domain which address is 0x20201048[0]	

5 Bus architecture

The bus architecture of RF03 is shown below.



The system bus is based on AHB and APB. The data width of the bus is 32 bits. The AHB bus works under the same frequency with CPU. The maximum frequency of AHB bus is 96MHz and programmable with 16MHz step. The maximum frequency of APB bus is one half of the frequency of AHB bus which is 48MHz. The frequency of APB bus is the integer division of the frequency of the AHB bus. There are altogether 4 AHB masters which are CPU, DMA, UART2AHB and CACHE. The exchange memory(EM/32KB) required by the BLE MAC is 32KB and shared with system SRAM. So the BLE MAC can access the SRAM directly through an internal interface. BLE MAC has the highest priority when any other AHB master accesses the same SRAM with BLE MAC at the same time. The accessibility and the priority of the AHB masters to the slaves is shown in the table below:

	BROM_CTRL	CACHE_MEM	SRAM_CTRL	OTHER	AWO_REG
CPU	0	0	1	0	0
UART2AHB	X	X	2	1	1
DMA	X	X	3	2	X
CACHE	X	X	X	X	X
BLE_MAC	X	X	0	X	X

In this table, X means the master can not access the slave. Number means the master can access the slave and 0 has the highest priority. The cache size in the bus diagram is 16kB which is shared with the system SRAM. When cache is enable, the last 16kB system SRAM address space must not be accessed by CPU or other bus master. The last 16kB SRAM is used as the cache SRAM at that time.

The size of the system SRAM is 208kB and the address starts with 0x100000. The system SRAM is composed of 7 sub SRAM blocks as described in chapter 4.5. And if one of the SRAM sub block is not needed any more in the system it can be powered of to save power. BLE_MAC can only access the fifth SRAM sub block which address starts with 0x128000. When the CPU is running on the external flash, the flash controller must be enabled and the last SRAM sub block is used as the cache and can not accessed by the other AHB master.

6 Address mapping

The address mapping of RF03 is shown below:

addr zone			start	end	space
brom			0x00000000	0x0001FFFF	128kB
reserved			0x00020000	0x000FFFFF	896kB
sram			0x00100000	0x00133FFF	208kB
reserved			0x00134000	0x001FFFFF	816kB
reserved			0x00200000	0x007FFFFF	6MB
cache			0x00800000	0x00FFFFFF	8MB
reserved			0x01000000	0x1FFFFFFF	496MB
reserved			0x20000000	0x200FFFFF	1MB
peripheral	ahb	ble_mac_reg	0x20100000	0x2010FFFF	64kB
		ble_mdm_reg	0x20110000	0x2011FFFF	64kB
		dma_reg	0x20120000	0x20120FFF	4kB
		cache_reg	0x20121000	0x20121FFF	4kB
		reserved	0x20122000	0x2012FFFF	56kB
	apb0	timer	0x20130000	0x20130FFF	4kB
		wdt	0x20131000	0x20131FFF	4kB
		sysc_bus	0x20132000	0x20132FFF	4kB
		bus_ptch	0x20133000	0x20133FFF	4kB
		ecc	0x20134000	0x20134FFF	4kB
		reserved	0x20135000	0x20135FFF	4kB
		reserved	0x20137000	0x2013FFFF	36kB
	apb3	uart0	0x20143000	0x20143FFF	4kB
		uart1	0x20144000	0x20144FFF	4kB
		iic0	0x20145000	0x20145FFF	4kB
		iic1	0x20146000	0x20146FFF	4kB
		pwm	0x20147000	0x20147FFF	4kB
		gpio	0x20148000	0x20148FFF	4kB
		sysc_per	0x20149000	0x20149FFF	4kB
		reserved	0x2014A000	0x2014FFFF	24kB
reserved			0x20150000	0x200FFFFF	704kB
awo	apb1	rtc	0x20200000	0x20200FFF	4kB
		sysc_awo	0x20201000	0x20201FFF	4kB

7 IO Mux

The IO mux table of RF03 is shown below.

pad		func0		func1			func2			func3			func4		
name	IO	sig_name	io	sig_name	io	en	sig_name	io	en	sig_name	io	en	sig_name	io	en
P00	B	swck	I	gpio[0]	B	gpio00_en									
P01	B	swd	B	gpio[1]	B	gpio01_en									
P02	B	gpio[2]	B		O					func_io[0]	B	func_io_en[0]			
P12	B	uart2ahb_txd	O	gpio[12]	B	gpio14_en	ble_mac_dbg[5]	O	ble_mac_dbg_en[5]	func_io[10]	B	func_io_en[10]	rfif_tx[2]	I	rfif_en
P13	B	uart2ahb_rxd	I	gpio[13]	B	gpio15_en	ble_mac_dbg[6]	O	ble_mac_dbg_en[6]	func_io[11]	B	func_io_en[11]	rfif_tx[3]	I	rfif_en
P15	B	gpio[15]	B							func_io[13]	B	func_io_en[13]	rfif_tx[5]	I	rfif_en
P16	B	gpio[16]	B							func_io[14]	B	func_io_en[14]			
P17	B	gpio[17]	B							func_io[15]	B	func_io_en[15]	rfif_tx[6]	I	rfif_en
P22	B	gpio[22]	B							func_io[20]	B	func_io_en[20]	rfif_tx[11]	I	rfif_en
P23	B	gpio[23]	B							func_io[21]	B	func_io_en[21]			

The programmable registers for the enable signals are listed below:

0x20132020[23:16]	ble_mac_dbg_en
0x20132020 [13]	rfif_en
0x20132020 [12]	gpio15_en
0x20132020 [10]	gpio01_en
0x20132020 [9]	gpio00_en
0x20132024[21:0]	func_io_en

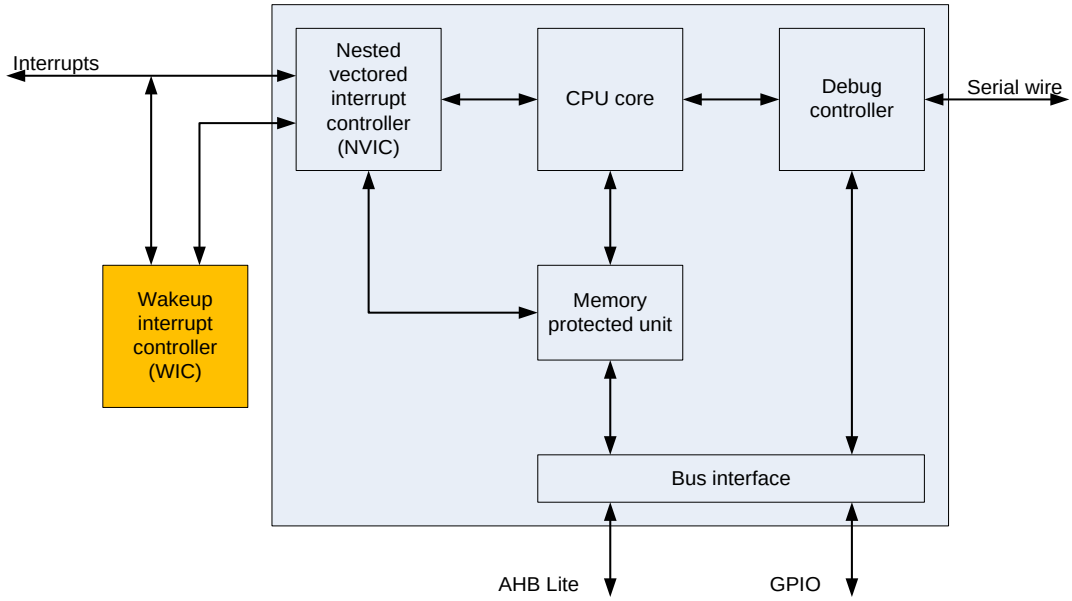
The func_io is shared by many interface modules and each bit of the func_io can be programmed to act as any of the shared function. The share table is listed below:

signal name	io	idx
uart0_txd	O	0
uart0_rxd	I	1
uart0_cts	I	2
uart0_rts	O	3
uart1_txd	O	4
uart1_rxd	I	5
iic0_scl	B	6
iic0_sda	B	7
iic1_scl	B	8
iic1_sda	B	9
pwm0	O	10
pwm1	O	11
pwm2	O	12
pwm3	O	13
pwm4	O	14

8 CPU

8.1 General description

RF03 integrates CPU. The processor is an ultra-low power 32-bit processor designed for a broad range of embedded applications. The block diagram of processor is shown below:



The processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The processor is based on the 16-bit Thumb instruction set and includes Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

The processer integrates a nested vectored interrupt controller, a debug controller and a memory protect unit.

9 Cache controller

9.1 Feature List

- Zero wait cycle when cache hit
- 8MB cachable address space with the start address programmable
- 16KB cache data size which is shared with the system SRAM
- Supports cache flush command
- 4 Way cache with LRU algorithm
- Read only cache
- 32 bytes cache line size

10 UART

10.1 Feature list

- 32 bytes transmit and receive FIFO
- Hardware flow control(UART0 only)
- IRDA 1.0 SIR mode support(UART0 only)
- Programmable baud rate
- Programmable frame format of data bits per frame
- Optional parity bit and programmable number of stop bits
- DMA transmission

11 IIC

11.1 Feature list

- Two-wire IIC serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Three speeds are supported: Standard mode (0 to 100Kbps); Fast mode (400Kbps) or High-speed mode (3.4Mbps)
- Master OR slave IIC operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- Transmit and receive FIFO
- Handles Bit and Byte waiting at all bus speeds
- Supports DMA transfer
- Programmable SDA hold time

12 Power management

The power management unit (PMU) in RF03 comprises a DC-DC Buck Converter, various LDOs for the different power domains of the system. The PMU is capable of supplying external devices even during RF03 in sleep mode.

Features

- DC-DC Buck Converter with excellent 93% efficiency
- Programmable DC-DC converter output charging sequence
- One LDO output up to 3.3 V with up to 50 mA load capability
- DC-DC converter automatically on/off control during in sleep mode
- Active and Sleep mode current limited LDOs
- Use of small external components
- Supply of external rails (V33, VDD1V8) while in Sleep mode

13 DC/DC Buck Converter

Two DC/DC Buck Converter modes are designed for RF03. One is DC/DC Converter ON and the other is DC/DC Converter Bypass. RF03 will automatically enter DC/DC Converter ON mode within 150 us while CPU is active. And DC/DC Converter will be bypass mode during CPU in sleep mode.

(Ta = -40℃ ~ +85℃, 2.3V ≦ VBAT ≦ 5V)

Item	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
DC/DC Converter	Input Voltage		2.3		4.75	V
	Output Voltage	DC/DC Converter On (Default 1.4V)		1.4		V
				1.3		V
				1.2		V
				1.1		V
		DC/DC Converter Bypass		VBAT-0.3		V
	Quiescent Current	DC/DC Converter On		100		uA
	Start-up Time	DC/DC Converter On		120		usec

14 LDO

RF03 provides several LDOs to external power supply, including two 3.3V LDO and one 1.8V LDO. The LDO for external use can be configured as active even in sleep mode. The LDO characteristics are listed below.

(Ta = -40℃ ~ +105℃, 2.3V ≦ VBAT ≦5.0V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
1.8V LDO	Output Current			40	mA
	Output Voltage at 96MHz > 10mA		1.8		V

(Ta = -40℃ ~ +105℃, 2.3V ≦ VBAT ≦5.0V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
3.0V LDO_1	Output Current			25	mA
	Output Voltage		3.0		V

Ta = -40℃ ~ +105℃, 2.3V ≦ VBAT ≦5.0V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
3.0V LDO_2	Output Current			50	mA
	Output Voltage		3.0		V

15 32MHz Crystal Oscillator

32MHz Crystal Oscillator characteristics are listed below. Also, frequency compensation, programmable level of frequency compensation capacitors will be implemented to cover 32MHz Crystal variation, aging … over temperature range -40℃ ~ +105℃.

(Ta = -40℃ ~ +105℃ , 2.3V ≦ VBAT ≦ 5V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
32MHz Crystal Oscillator	Oscillation frequency		32		MHz
	Frequency offset	-20		20	ppm
	Startup time			150	μs
	Shunt Capacitor (with NDK NX3225SA)			10	pF

16 32MHz RC Oscillator

32MHz RC Oscillator characteristics are listed below.

(Ta = -40℃～+105℃，2.3V ≦ VBAT ≦ 5V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
Internal 32MHz RC Oscillator	Oscillation frequency		32		MHz
	Startup time		-	20	μs

17 32KHz Crystal Oscillator

32KHz Crystal Oscillator characteristics are listed below.

(Ta = -40℃～+105℃，2.3V ≦ VBAT ≦ 5V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
32.768KHz Crystal Oscillator	Oscillation frequency		32.768		KHz
	Frequency offset	-20		20	ppm
	Series Resistor		10		MΩ
	Shunt Capacitor		33		pF

18 32KHz RC Oscillator

32KHz RC Oscillator characteristics are listed below

(Ta = -40℃～+105℃，2.3V ≦ VBAT ≦ 5V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
Internal 32KHz RC Oscillator	Oscillation frequency		32		KHz
	Frequency offset after calibrated by 32MHz Crystal Oscillator	-500		500	ppm
	Chip-to-chip Variation from -40℃～+85℃，2.3V～5V	10	-	100	KHz

19 PLL

RF03 provides alternative 96/80/64/48/32/16 MHz system clock. Changing this system's clock can be done within 300 us without affecting the operation of the chip. This PLL dissipates additional 0.4 mA when operating at 96 MHz.

(Ta = -40℃ ~ +105℃, 2.3V ≦ VBAT ≦ 5V)

Item	Parameter	MIN.	TYP.	MAX.	Unit
PLL	Output Clock (Default 96MHz)		96		MHz
			80		MHz
			64		MHz
			48		MHz
			32		MHz
			16		MHz
	Reference Clock		16		MHz
	Stable time			300	μs