

BlueX Microelectronics Co., Ltd.

Bluetooth 5.0 LE | MESH SoC

System Installation of

Evaluation Kit

BX2400-dRF0xp-S1x

BX2400-eRF01e-G1x

Version 1.7

Aug. 11th, 2021 released



http://www.bluexmicro.com



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1. Evaluation Kit Introduciton

In this section, we'll introduce the function and usage of each EVK, and diagram attached at the end of each paragraph.

1.1 EVK of BX2400-dRF0xp-S1c

This EVK is applicable to all BlueX BLE chips except RF01. Items (1) to (18) will be introduced as below.



- (1) USB Type C Connector
 - A. USB 5V power input.
 - B. It provides USB to convert to UART, and links to UART(P12/P13) connector on module.
- (2) Primary Power Switch
 - Please compare with #9, secondary power switch. Status listed as below:

#2 Switch	#9 Switch	EVK Power	Module Voltage
Up	Up	2ea AA batteries	3.0V
Down	Up	2ea AA batteries	3.0V
Up	Down	DC 5V from #3	4.2V
Down	Down	DC 5V from USB	4.2V

According to operating voltage ranging from 2.3V to 3.6V, please be noticed it can only be using 2ea AA batteries when BX2416 module on EVK.

(3) D5V External Power Connector

A. External power input port, DC 5V.

- (4) RF0x Module Power Connector
 - A. Module power output connector, available for outputting power for external circuit.
 - B. When EVK using USB power or D5V, here it outputs 4.2V.
 - C. When EVK using 2ea AA batteries, here it outputs from batteries.
- (5) IO Expanding Connector
 - A. RF0x Module IO and power expanding connector.



- (6) Module Adapter Board
 - A. When BX2416/ RF03/ RF04/ RF08 modules welded on adapter board, plug in here on the EVK as below:



- (7) RF04/ RF08 Module Welded Area
 - A. RF04/ RF08 Module can be welded here on the EVK.
- (8) Buzzer
- (9) Secondary Power Switch

Please refer to #2, primary power switch, for comparison.

- (10) RGB LED
- (11) RF0x Module Reset Button
 - A. Press this button to reset chip on module.
- (12) OLED Display Screen
- (13) LIS3DSH Acceleration Transducer Connector
- (14) P16/ P23/ Watchdog DIP Switch

#14 Switch			Description		
			BOOT Pin of chip. Chip activated from UART0 P12(TX)/		
Left P16		Up	P13(RX) for firmware download.		
		Down	Chip activated from Flash.		
Mid	220	Down	When using chips RF08 on module, switch this down		
		DOWI	before power-on.		
Lin		lln	Watchdog timeout period is around 25sec, and module		
Diaht	Watchdog	υp	will reset afterwards.		
RIGHT	watchdog	Down	Switch down when no using it. If there's no Watchdog IC		
		DOMI	welded on EVK, no need to concern this switch.		

- (15) Circuit Connector (P10/ P11/ P21)
 - A. P10 for RGB LED green, or DC pin from OLED display screen.
 - B. P11 for RGB LED blue, or RST pin from OLED display screen.
 - C. P21 for RGB LED red, or QD pin from humidity sensors.
- (16) DS18B20 Humidity Sensors Connector
- (17) UART Connector
 - A. Connect to RF0x UART P12/ P13 connector.
- (18) SWD Connector
 - A. J-Link SWD debugging connector for RF0x module programming and softeare debugging.



1.2 EVK of BX2400-eRF01e-G10

This EVK is applicable to RF01. Items (1) to (11) will be introduced as below.



- (1) RF01, QFN52, 6*6mm
- (2) External Antenna Mount
- (3) Power Supply 3.3V LDO
- (4) Jumper Terminal
 - A. Separate VDD_BAT and LDO. If unplugged, VDD_BAT and 3.3V LDO are disconnected, using for checking overall power consumption current.
- (5) Battery Terminal
 - A. VDD_BAT on the left, GND on the right.
 - B. Should be in alliance with items#4. When connected #4, battery supplies RF01 through LDO. When not connected, battery supplies RF01 directly.
- (6) IO External Connector: pinout as below





- (7) SWD Debugging Connector
 - A. P00-SWCLK, P01-SWDIO
- (8) UART Serial Connector
 - A. P12-TXD, P13-RXD
- (9) P16/P23 DIP Switch
 - A. P16 on the left, P23 on the right.
 - B. Same as EVK of BX2400-dRF0xp-S1a. Please refer to #14 in paragraph 1.1 above.
- (10) Button and LED
 - A. KEY-P15/P17, LED-P02/P03. No special default and it's configuarable for user.
- (11) SPI Flash IC
 - A. CS#-P24, DO-P27, WP#-P28, HOLD#-P29, CLK-P25, DI-P26.



1.3 EVK of BX2400-eRF01e-G1a

This EVK is applicable to RF01. Items (1) to (10) will be introduced as below.



- (1) RF01, QFN52, 6*6mm
- (2) External Antenna Mount
- (3) RGBW LED
 - A. IO connect as below:



- (4) IO External Connector
 - A. Pinout as below



B. VDD_3V_0 means 3.3V LDO output, power supply for RF01 VDD_BAT/1/2 PIN.



(5) Power, IO, and SWD connect as below:



- A. Pin#15 and Pin#16 are RF01 SWD interface, using for debug and FW download.
- (6) SPI Flash

A. CS#-P24, DO-P27, WP#-P28, HOLD#-P29, CLK-P25, DI-P26.

- (7) Power Supply 3.3V LDO.
- (8) P16/P23 DIP Switch
 - A. P16 on the left, P23 on the right.
 - B. Same as EVK of BX2400-dRF0xp-S1a. Please refer to #14 in paragraph 1.1 above.
- (9) Button
 - A. IO connect as below:



(10) Type-C USB Connector

- A. USB 5V power input.
- B. It provides USB to convert to UART, and links to UART(P12/P13) connector on module.



1.4 IO Introduction

- (1) IO
 - A. P00 to P29 are digital IO, available for GPIO.
 - B. P30 to P35 are analog input, not available for GPIO.
 - C. P00 and P01 are linked to SWCLK and SWDIP of J-Linkrespectively.
- (2) UART
 - A. P12 and P13 are TX and RX of UARTO respectively.
- (3) SPI
 - A. Supports SPI 2 channels at the most, and pins of SPIM and SPIS are fixed when processing.
 - B. SPIMO uses P02(CS1), P03(CS0), P04(CLK), P05(MISO), and P06(MOSI).
 - C. SPIM1 uses P07(CS1), P08(CS0), P09(CLK), P10(MISO), and P11(MOSI).
 - D. SPIS uses P03(CS), P04(CLK), P05(MISO), and P06(MOSI).
- (4) I²C
 - A. Equipped with I²C 2 channels, configuration available from PO2 to P23.
- (5) PWM
 - A. Supports PWM 5 channels at the most, configuration available from P02 to P23.
- (6) ADC
 - A. Supports 6 channels of ADC data acquisition at the most. Independant analog IO of each(P30 to P35).
- (7) External Interrupt
 - A. P15, P16, P17, P22, and P23 are external interrupt pins to support wake-up from sleep mode.





2. Tools Download

Please download the version of Keil 5.0 and J-Link 6.3 at least.

3. Tools Installation

- 3.1 Keil Installation
 - (1) Click the installation.

名称	*	修改日期	关型	大小
🛃 JLink_Windows_V646j		2020/2/4 13:40	应用程序	35,369 KB
		2020/2/4 14:13	好压 RAR 压缩文件	530 KB
🛃 mdk523		2020/2/4 15:55	应用程序	737,407 KB

(2) Click [Next].

Welcome to Keil MDK-ARM Release 2/2017	ARM [®] KEIL [®] Microcontroller Tools
This SETUP program installs:	
MDK-ARM V5.23	
This SETUP program may be used to update a previous However, you should make a backup copy before proce	product installation. eding.
It is recommended that you exit all Windows programs be	fore continuing with SETUP.
Follow the instructions to complete the product installation	n
Kell MDK-ARM Setup	

(3) Check [I agree all the terms of the preceding License Agreement], then click [Next].

License Agreement Please read the following license agreement carefully.	ARM [®] KEIL Microcontroller Tools
To continue with SETUP, you must accept the terms of the Lice agreement, click the check box below.	ense Agreement. To accept the
THIS END USER LICENCE AGREEMENT FOR MDR-ARM BETWEEN YOU (EITHER A SINGLE INDIVIDUAL, OR ARM LIMITED ("ARM") FOR THE USE OF THE SOFT	E") IS A LEGAL AGREEMENT SINGLE LEGAL ENTITY) AND WARE ACCOMPANYING THIS HE SOFTWARE TO YOU ON
LICENCE. ARM IS ONLY WILLING TO LICENSE T CONDITION THAT YOU ACCEPT ALL OF THE TO CLICKING "I AGREE" OR BY INSTALLING OR OTHE	ERMS IN THIS LICENCE. BY ERWISE USING OR COPYING -



(4) Select the destination and click [Next].

older Selection Select the folder where SETUP will install files.	ARM KEIL Microcontroller Tools
Press 'Next' to install MDK-ARM to these folders. Press 'Browse' t	to select different folders for installation.
Pestination Folders	
Core: [C:\Keil_v5	Browse
Pack: [C:\Keil_v5\ARM\PACK	Browse
Cal MDK ARM Setur	

(5) Fill in information and click [Next].

Please enter your name, the name of the company for whom you work and First Name:	d your E-mail address.
First Name:	
Last Name:	
Company Name:	
E-mail:	

(6) Wait for installing.

Setup Status	ARM KEIL Microcontroller Tools
MDK-ARM Setup is performing the requ	ested operations.
Install Files	
Installing c_we.b.	
Keil MDK-ARM Setup	



(7) Click [Finish] when it completes.



3.2 Environment Variables Setting

(1) Right-click on [My computer] and choose [Properties].



(2) Choose [Advance System Settings].

🔜 System		– 🗆 X
← → · ↑ 🗹 > Control P	anel > All Control Panel Items > System	v さ Search Co ク
Control Panel Home	View basic information about your computer	0
💡 Device Manager	Windows edition	
Remote settings	international sectors and the	
System protection	Contraction in process	Windows10
	System	
	Processor: Installed memory (RAM):	
	System type:	
	Pen and Touch:	
	Computer name, domain, and workgroup settings	
	Computer name:	Change settings
	Full computer name:	
	Computer description:	
	Workgroup:	
	Windows activation	
	the second se	Change product key
		• • • •
See also		
Security and Maintenance		
-		



(3) Click [Enviroment Variables].



(4) Choose [Path] and then click [Edit].

Variable	Value
MGLS LICENSE FILE	C:\MentorGraphics\LICENSE.DAT
MOZ PLUGIN PATH	C:\Program Files (x86)\Eoxit Software\Eoxit Reader\plugins\
OneDrive	C:\Users' OneDrive
OneDriveConsumer	C:\Users' OneDrive
Path	C:\Users\ \AppData\Local\Microsoft\WindowsApps;;C:\Ment
SRFPROG2	C:\Progr (x86)\Texas Instruments\SmartRF Tools\Flash Prog
TEMP	C:\Users
stem variables	New Edit Delete
rstem variables Variable	New <u>£</u> dit <u>D</u> elete
rstem variables Variable PADS PROGRAMS	New Edit Delete
rstem variables Variable PADS_PROGRAMS PADS_ROOT	New Edit Delete Value Programs C\MenterGraphics\9.5PADS\SDD HOME
rstem variables Variable PADS_PROGRAMS PADS_ROOT Path	New Edit Delete Value Programs C:\MentorGiraphics\9.5PADS\SDD HOME C:\ProgramData\0racle\Javajavapath;C:\Program Files (i:86)\Com]
rstem variables Variable PADS_PROGRAMS <u>PADS_ROOT</u> Path PATHEXT	New Edit Delete Value Programs C:\MentorGraphics\9.5PAD5\SDD HOME C:\ProgramData\Oracle\Java\javapath;C:\Program Files (x86)\Com COM_EXE;BAT;.CMD;VBS;,VBE;JS;JSE;WSF;WSH;MSC
rstem variables Variable PADS_PROGRAMS PADS_ROOT Path PATHEXT perfinterp	New Edit Delete Value Programs C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\DD_HOME
Istem variables Variable PADS PROGRAMS PADS ROOT Path PATHEXT perlinterp PROCESSOR_ARCHITECTURE	New Edit Delete Value Programs C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME C:\MentorGraphics\9.5PADS\SDD_HOME M:\mathcal{Bit} A:\mathcal{Bit} A:\mathcal{Bit}
Istem variables Variable PADS_PROGRAMS PADS_ROOT Path PATHEXT perlinterp PROCESSOR_ARCHITECTURE PROCESSOR_ARCHITECTURE PROCESSOR_ARCHITECTURE	New Edit Delete Value Programs C:\MentorGraphics\9.5PADS\SDD HOME C:\MentorGraphics\9.5PADS\SDD HOME C:\ProgramData\0racle\Javajavapath(C:\Program Files (x86)\Com) .COM, EXE;BAT;.CMD; VBS; VBE;JS;JSE;WSF;WSH;MSC C:\MentorGraphics\9.5PADS\SDD_HOME\common\win32\perl\bin AMD64 AMD64 Family 23 Model 8 Steoping 2. AuthenticAMD . .

(5) Choose bin file under Keil, and click [OK] to set.

C:\ProgramData\Oracle\Java\javapath	New
C:\Program Files (x86)\Common Files\Oracle\Java\javapath	
C:\MentorGraphics\9.5PADS\SDD_HOME\common\win32\bin	Edit
C:\MentorGraphics\9.5PADS\SDD_HOME\common\win32\lib	
%MGC_HOME%\bin	Browse
%MGC_HOME%\lib	
C:\Program Files (x86)\NVIDIA Corporation\PhysX\Common	<u>D</u> elete
%SystemRoot%\system32	
%SystemRoot%	
%SystemRoot%\System32\Wbem	Move <u>Up</u>
%SYSTEMROOT%\System32\WindowsPowerShell\v1.0\	
%SYSTEMROOT%\System32\OpenSSH\	Move Down
C:\Keil_v5\ARM\ARMCC\bin	
	Edit text
	_
	-

(6) Click [Confirm] and complete environment variables setting.



3.3 J-Link Installation

(1) Click the installation.

名称	修改日期	类型	大小
Link_Windows_V646j	2020/2/4 13:40	应用程序	35,369 KB
	2020/2/4 14:13	好性 KAR 法殖文件	530 KB
ndk523	2020/2/4 15:55	应用程序	737,407 KB

(2) Click [Next].



(3) Click [I Agree].

SEGGER - J-Link V6.40	ij Setup License Agreement Please review the license terms before installing SEGGER - J-Link V6.46j.	J Link
Stand Lar	Press Page Down to see the rest of the agreement.	
Embedded Studio	Important - Read carefully: DEFINITIONS: For the purpose of this agreement, the terms shall have the following meaning when the entire word is marked bold: The "software" means all J-Link related software components included in the J-Link.	Î
Powerful C/C++ IDE available for Windows macOS Linux	the "/www.sequer.com/link-software.html the "/www.sequer.com/link-software.html "Licensor" shall mean SEGGER except under the following circumstances: If you accept the terms of the agreement, click I Agree to continue. You must accept the agreement to install SEGGER - J-Link V6.46j.	•
Download Trial	< Back I Agree Can	cel

(4) Click [Install]. Please install it in the default destination and DO NOT revise.

SEGGER	Choose optional components Choose optional components to be installed.
IoT 🔊	Install USB Driver for J-Link Create entry in start menu Add shortcuts to desktop
AUBA	Choose destination: Update existing installation Install a new instance
Discover SEGGER solutions for the Internet of Things	C: Program Files (x86) \SEGGER \JLink Browse
Learn More	< Back Install Cancel



(5) Wait for installing.

J-Trace	Extract: JLink_x64.dll 87%	
	Extract: JLinkRTTLogger.exe Extract: JLinkRTTViewer.exe Extract: JLinkRedistration.exe	
J-Trace PRO	Extract: JLinkRemoteServer.exe Extract: JLinkRemoteServerCL.exe	
Trace and Debug in Real Time!	Extract: JLinkSTM32.exe Extract: JLinkSTR91x.exe Extract: JLinkSWOViewer.exe	
 Streaming Trace Live Profiling Code Coverage 	Extract: JLinkSWOViewerCL.exe Extract: JLink_x64.dll 87%	-

(6) Click [Finish] to complete.







4. J-Link Introduction

J-Link firmware should be version 6.0 at least, and hardware should be version 9.0 at least.

4.1 Procedure Programming

Taking SDK 3.x for example, download link as below: https://www.bluexmicro.com/download/cid-6.html

- (1) Option 1: Download by J-Flash
 - A. Find [BlueX] file and [JLinkDevices.xml] under path of [SDK3\tools\bluex\prog_tool_v2] as below.

	> SDK3 > tools > blu	K3 > tools > bluex > prog_tool_v2							
名称 ^	修改日期	类型	大小						
BlueX	2021/3/8 14:08	文件夹							
JLinkDevices.xml	2021/1/4 16:35	XML 文档	1 KB						
ReadMe.txt	2021/1/4 16:35	文本文档	1 KB						

B. Copy [BlueX] file and [JlinkDevices.xml] to J-Link file as below.

		_		
	SEGGER > JLink	_V644		
名称 ^	修改日期	类型	大小	
BlueX	2021/5/26 17:04	文件夹		
Devices	2020/4/25 15:23	文件夹		
Doc	2020/4/25 15:23	文件夹		
ETC	2020/4/25 15:23	文件夹		
GDBServer	2020/4/25 15:23	文件夹		
RDDI	2020/4/25 15:23	文件夹		
Samples	2020/4/25 15:23	文件夹		
USBDriver	2020/4/25 15:23	文件夹		
🔜 JFlash.exe	2019/4/12 23:18	应用程序	704 KB	
🔜 JFlashLite.exe	2019/4/12 23:18	应用程序	345 KB	
🛃 JFlashSPI.exe	2019/4/12 23:18	应用程序	408 KB	
🛃 JFlashSPI_CL.exe	2019/4/12 23:18	应用程序	563 KB	
🔜 JLink.exe	2019/4/12 23:18	应用程序	292 KB	
🗟 JLink_x64.dll	2019/4/12 23:19	应用程序扩展	17,268 KB	
🗟 JLinkARM.dll	2019/4/12 23:18	应用程序扩展	16,184 KB	
🔜 JLinkConfig.exe	2019/4/12 23:18	应用程序	441 KB	
JLinkDevices.xml	2021/4/15 11:09	XML 文档	1 KB	



(A) If there's already [JLinkDevices.xml] file under J-Link, please follow steps as below. First, click [JLinkDevices.xml] file under SDK3.x. Then, copy content of Device inbetween.



(B) Third, open [JLinkDevices.xml] file from J-Link, and paste it above </DataBase>.





C. Click

to open J-Flash V6.44f and click [File] to choose [New Project] as below.





D. In [Create New Project], click the button indicated by red arrow as below.

Target Device		
Cortex-M0		
Little endian 💌		1
Target Interface	Speed (kHz)	
SWD 🗸	4000	•

E. Roll down to choose [BlueX].

lanufacturer ×		•			
Manufacture Abov	/	^	Core	Flash size	RAM size
Inspecified activ	e-semi		ABM7		
Inspecified Alter	a		ABM9		
Inspecified Amb	idWicto		ABM11		
Inspecified Ams			Cortex-A5		
Inspecified Amai	J		Cortex-A7		
Inspecified AuD	aeKau		Cortex-A8		
Inspecified Blue	X		Cortex-A9		
Inspecified Cirru	sLogic		Cortex-A12		
Inspecified Cypr	ess		Cortex-A15		
Inspecified Dialo	a Semiconductor		Cortex-A17		
Inspecified Digi	-		Cortex-A53		
Inspecified DSP	Group		Cortex-A57	2 C	
Inspecified Epso	n		Cortex-M0		
Inspecified Fara	day		Cortex-M0		
Inspecified Giga	Device		Cortex-M1		
Inspecified Hilso	her		Cortex-M3		
Inspecified Int	sk.	~	Cortex-M4	1	
Inspecified	Lortex-M7	•	Cortex-M7		
Inspecified	Cortex-M23		Cortex-M23		
Inspecified	Cortex-M33		Cortex-M33	2 C	
Inspecified	Cortex-R4		Cortex-R4	2	
Inspecified	Cortex-R5		Cortex-R5		
Inspecified	Cortex-R8		Cortex-R8		
Inspecified	RX		BX		
Inspecified	RISC-V		RISC-V		
hov	AC33M6128		Cortex-M3	128 KB	12 KB

F. Choose program according to Module Flash voltage, then click [OK]. Choose [Apollo_00_3V3] when using RF01/RF03/RF04/BX2416/BX2417/BX2418 Module, or [Apollo_00_1V8] when using RF08.

aumacunet (Bine)	· ·			
Manufacturer	Device	Core	Flash size	RAM size
llueX llueX	Apolo_00_1V8 Apolo_00_3V3	Contex-MD Contex-MD	8192 KB 8192 KB	160 KB 160 KB



G. Back to [Create New Project] to choose [4000kHz] and click [OK].

Create New Project		×
Target Device		
BlueX Apollo_00_1V8		
Little endian 💌		
Target Interface	Speed (kHz)	
SWD 💌	4000	-
		<u>0</u> K

H. When configuration completed, click [File] then [Open data file] to select the firmware in hex file to download.



I. After selection, J-Flash will be as below.

Eile Edit View	ash V6.44f - [new projec / Target Options W	t*] Indow Help													-	_		×
Project - net	v p	Address: 0	×800000			×1 ×2	× <u>4</u>							DK3	example			×
Target interface Init SWD speed SWD speed	SWD 4000 kHz 4000 kHz BlueX Apollo_00_1V8	Address 800000 800010 800020 800030	0 1 42 58 00 00 B0 B5 DB 00	2 32 04 69 CB	3 34 00 46 1A	4 5 00 80 00 00 42 78 9D 46	6 12 07 00 05	7 8 00 1 00 0 AF 9 00 6	8 9 C 14 8 00 2 06 9 46	A 00 3B 92 00	B 00 60 0F 78	C 1 19 8 35 1 D3 1 01 F	D E 2 12 1 01 D DI 0 81	F 00 29 08 F9	ASCII BX24 iFBx.	;` iF.>	5>	
Endian Check core ID Use target RAM Flash memory Base address Clash size	Lottex:MU Little No 192 KB @ 0x100000 Internal bank 0 0x800000	800040 800050 800060 800070 800080 800080	07 21 98 40 F8 B9 DB 00 4E FI 06 30	01 A2 6A D3 07	20 5C 46 1A 22 40	6B 78 BD 46 44 78 9D 46 6B 78 28 78	6C 10 00 05 6E 72	46 1 40 4 AF A 00 2 46 1	B 07 3 1E 4 06 2 00 B 07 9 46	1B 98 A4 00 1B 22	0F 41 0F 21 0F 0F	DA 1 CØ E E3 1 68 4 D9 1	0 01 2 B0 D D1 6 D5 0 13	40 BD 08 F6 40 F9	.!. kxl .0.\.F. jFDx. F. N''kxr	LF .@CA 	e	
Flash size	8192 KB	8000A0 8000A0 8000B0 8000C0 8000D0 8000E0	BD 46 62 68 04 94 14 00 11 F9	F8 20 12 00 00	40 BD 68 00 F0 1B	28 78 10 B5 00 21 0C 94 F3 F8 43 42	72 06 D9 12 01 58	4C 0 F6 3 00 7 20 3 41 C	7 46 6 4B 2 FD 0 B5 2 00 8 B2	22 9C 08 05 29 70	42 34 00 00 BD	00 D F4 E 07 4 40 4 B7 1	0 63 3 10 7 C0 8 01 2 00 D C1	F7 BD 46 600 F0 604	.F	.L.K.E 24 p . 2.). (Ap.	F F H .@B	
		8000F0 800100 800110 900120	80 21 49 00 3C 4H	F0 00 9A	B5 93 42 10	3F 4B 01 F0 4C D1 55 57	40 84 3C 109	4C 1 F8 3 4B 3	B 69 C 4B C 48 A 20	85 3D 2B 55	BØ 4D 60 50	22 Ø 22 6 ØØ 9	0 18 8 21 B 62	00 60 68 40		DL.i. <k=m (K<h+)< td=""><td>"bh bh</td><td>•</td></h+)<></k=m 	"bh bh	•
- J-Flash V6.4 - JLinkARM.dll Opening project - Project open Failed to open Close project - Project clos Creating new pr	Proce Image: Second secon																	
- New project Opening data fii - Data file op < Ready	creat 3 E-13. Le enea succes.																	>



J. Connect EVK through J-Link SWD connector, and click [Target] to choose [Connect].

SEGGER J	Flash V6.44f - [new proje	ct *]																	-		×
<u>F</u> ile <u>E</u> dit <u>V</u> i	w <u>Target</u> Options <u>V</u>	<u>V</u> indow <u>H</u> elp																			
Project - r	Connect			18	*科\女	欠件相	l¥\s		вхм	icro-	SDK:	3-rel	ease	-v3.2	-202	1010	04\SI	DK3\	example		×
Name	Disconnect			10		_	_1	-2	ut l											(_
Host connectio	Test		>	Ē	2	3	4	<u>~</u>	<u>~</u>	2	8	9	۵	B	c	n	F	F	ASCIT		
Target interface	Production Prog	gramming F	7	8	32	34		80	12	00	10	14	00	00	19	82	12	00	BX24		-11
SWD speed	Manual Program	nming	>	90	04	00	00	00	07	00	08	00	3B	60	35	11	01	29		;`5)	
HOU	División de la constante	000020		₽22	69	46	42	78	00	AF	92	06	92	ØF	D3	1D	DB	08	iFBx		
Core	BlueX Apollo_00_1V8 Cortex-M0	800030	DB	00	CB	18	9D	46	05	00	69	46	00	78	01 D	FØ	8E	F9	F	iF.×	
Endian	Little	800040	07	21	01	20	PB PB	78	60	46	18	07	18	ØF	DH	10	0B DO	40		······································	
Check core ID	No 102 KB @ 0-100000	800050	78	40 DC	HZ	50	BD	46	10	40 0 E	43	11	98	41 0E	50	1 D	PD BØ	BD	.e.\.F.e	GH	
Use target hair	132 KB @ 0x100000	000000	LO DD	00	вн	10	99 0 D	46	99	HL DO	22	00	00	24	E3 69	10	DB	EQ0	Jrbx	LP	
Flash memory	Internal bank 0	000070	AE	ED	03	23	60	70	65	46	10	69	1 D	0P	na	10	12	40	N Where I		
Base address	0x800000	000000	9E	20	00	40	20	70	10	10	10	40	10	or	01	TO TO	13	70	· · · · · · · · · · · · · · · · · · ·	200 2	
Flash size	8192 KB	000070	90 DD	31	71	40	10	DE	66	40	07	40	22	42	00	re D3	107	F 7	E I	IF	
		Seeene	עם د 2	40	20	60	10	21	na	40 RC	22	PD PD	70	24	00 74	23	10	46	.r	2 4 E	
		800060	02 04	00	12	00	80	04	12	60	70	DE	00 OE	94	67	40	OF.	90	DA A.:	24r v U	
		800000	14	99	12	EG	50	74	81	20	22	88	20	00	40	40	0E	DO DO		2	
		800000	14	50	00	10	43	42	E 0	41	52	89	27	DD	40	42	00	F0	CDVA	2.7.00	
		000010	11	6.1	100	1D	45	42	20	41	10	60	10	na	00	10	10	04		· · · p · · · · ·	
		0000100	40	61 00	10	60	31	TD	-10	70	1.0	407	20	40	22	00	70	60		(N-MUL.)	
		000100	47	40	80	73	40	ГØ D1	20	TO AD	30	40	20	40	22	00	2 D ()	60	/W DI /N	(N-M-N-	
		000110	36	4B 60	7H	10	40	בע פים	36	4B PP	36	70	2 B E E	00	90	7.8	20	08 410	/w.gp.()	10. TT	-
															0.14						

K. When connection success, it will be as below.

SEGGER J-Fl	ash V6.44f - (new projec	t*]																		-		×
<u>File E</u> dit <u>V</u> iew	/ <u>Target</u> Options <u>W</u>	(indow <u>H</u> elp																				
🔝 Project - net	w p 🗖 🗖 🔀	E:\BULEX	لا_2	て档済	料\\$	7件相	送/S	DK\E	зхмі	cro-	SDK	8-rel	ease	-v3.2	2-202	21010	04\SI	DK3\	example	• 😑		×
Name	Value	A <u>d</u> dress:	0x800	0000			×1	x2	×4													
Hust connection	USB [Device 0]	Address	0	1	2	3	4	5	6	7	8	9	A	B	С	D	E	F	ASCII			
Target interface	SWD	800000	42	58	32	34	00	80	12	00	10	14	00	00	19	82	12	00	BX24.			
Init SWD speed	4000 kHz	800010	00	00	04	00	00	00	07	00	08	00	3B	60	35	11	01	29			: '5)	
SWD speed	4000 KH2	800020	BØ	B5	69	46	42	78	00	AF	92	06	92	ØF	D3	1 D	DB	08	iFB	×		
MCU	BlueX Apollo 00 1V8	800030	DB	88	CB	18	9D	46	Ø5	RЯ	69	46	00	78	Ø1	FØ	8F	F9		F iF	7 x	
Core	Cortex-M0	800040	07	21	R 1	20	6 R	78	60	46	1 R	87	18	ØF	ΠÓ	10	ØR	40	• •	v1F	6	
Endian	Little	900050	00	40	02	50	Ph	46	10	40	42	11	90	41	CR	10	PR	PD		F GC		
Line target RAM	N0 192 KR @ 0-100000	000050	10	DC	60	46	44	70	00	00	-13	86	04	0P	E.3	10	DD	60		r.eo.		
Use target hmm	132 KB @ 0x100000	000000	PD DD	85	D2	10	44	40	00	nr	22	00	00	01	60	10	DD	DO DC	•••JFD	×	• L.F	
Flash memory	Internal bank 0	000070	AE	ED	07	711	7D CD	10	605 6 E	46	4 D	60	100	21 0F	D0	10	12	10	 м. ул.	F	nr	
Base address	0x800000	000000	46	70	00	40	00	70	00	10	10	40	10	or	07	10	13	40	HK	xnr		
Flash size	8192 KB	800070	00	3H	28	40 DD	28	78	66	54	63	40 4D	22	40	90	PO	67	F9 DD		xriir	·1.	
		800000	BD	46	F8	RD	10	R2	ØБ	40	ЮЬ	48	90	42	99	D3	10	RD	.F		с.в	
		800080	62	68	20	68	00	21	DA	F6	32	FD	68	34	F4	EA	CN	46	bh h.	•	.4	, i i
		800000	04	94	12	00	ØC	94	12	00	70	B 5	05	00	07	48	ØE	00		· · · p.	· · · · H · ·	
		800000	14	00	00	FØ	F3	F8	01	20	32	00	29	00	40	42	00	FØ		2.	.>.@B	
		8000E0	11	F9	00	1B	43	42	58	41	CØ	B2	70	BD	B7	1D	C1	04	C	BXA	p	
		8000F0	80	21	FØ	B5	3F	4B	40	4C	1B	69	85	BØ	22	00	18	00	. • ?	K@L.i	ι"	
		800100	49	00	00	93	01	FØ	84	F8	3C	4 B	3D	4D	22	68	2B	60	I	<Ж	(=M''h+`	
		800110	30	4 B	9A	42	4C	D1	3C	4 B	3C	48	2B	60	00	9B	62	68	<k.bl< td=""><td>.<x<h< td=""><td>I+`bł</td><td></td></x<h<></td></k.bl<>	. <x<h< td=""><td>I+`bł</td><td></td></x<h<>	I+`bł	
,		000120	01	20	10	10	DD	60	ħØ	DD	90	20	C.C.	ħΑ	00	00	20	AD	h		·^	
LOG																						83
- FPUnit: 4 co	de (BP) slots and O lit	eral slots																				^
- CoreSight co	mponents: ROOFFOOO																					
- ROMTL1[0][0]	: E000E000, CID: B105E0	OD, PID: OOOBB	008 3	SCS																		
- ROMTL1[0][1]	: E0001000, CID: B105E0	OD, FID: COOBB	OOA I	TWC																		
- Executing in	it sequence	<i>bb, 11b. 000bb</i>	. 000																			
- Initializ	ed successfully																					
- T-Lish found	1 JTAC Lunice. Core ID	: 0x0BC11477 (None)																			
-Connected su	ccessfully																					
1																						
																						·
Ready												C	onn	ected	ł	Cor	e Id	: 0x0	BC1147	7 Spe	eed: 4000) kH 🧷
							-	_			_			-								

L. Click [Target] to choose [Produciton Programming] to download firmware.

SEGGER J-Fl	ash V6.44f - [new projec	t *]																_	C]	×
File Edit View	V Target Options W	indow Help	_																		
Rroject - ne	Connect		资料	斗∖软件	相关\		зхмі	cro-	SDK	B-rel	ease	-v3.2	2-202	21010	D4\SI	DK3\	examp	ole	-		×
Name	Disconnect		20		Jul 1																
Host connection	Test	>	E.	0 0	1×1	<u>×</u> .	<u>×</u>		0	0	•	n	0	n	F		0001				ы
Target interface	Production Prog	ramming F7	1	2 3 32 34	4 100	5 80	ь 12	7 00	8 1C	9 14	н 00	в 00	19	82	12	г 00	BX24	1			-9
Init SWD speed SWD speed	Manual Program	nming >	90	04 00	00	00	07	00	08	00	3B	60	35	11	01	29			;`!	;)	
		000020 10	-35	69 46	5 42	78	00	AF	92	06	92	ØF	D3	1D	DB	08	iF	B×	• • • • •	• • • •	
мсо	BlueX Apollo_00_1V8	800030 DB	00	CB 16	9 P	46	05	00	69	46	00	78	01	FØ	8E	F9		.F	iF.×.		
Lore	Lortex-MU	800040 07	21	01 20	0 6B	78	6C	46	1B	07	1B	ØF	DA	10	ØB	40		kx1F		e	
Englan Charles and ID	Little	800050 98	40	A2 50	: RD	46	10	40	43	1 E	98	41	СЙ	B 2	RØ	BD		F.P	C A		
Lineck core ID	102 KB @ 0-100000	9000C0 T0	DE	60 40	: 44	70	00	AP	0.4	<u>ac</u>	04	ar	E2	10	DB	00	417				
Use target hAM	132 KB @ 0x100000	000000 10	БЭ	OH 40) <u>44</u>	10	99	нг	H-4	90	нч	or	£Э	10	DP	60	Jr	DX			
Elsek menen	Internal bank 0	800070 DB	00	D3 16	1 9D	46	05	00	22	00	00	21	68	46	D9	F6		.F	"!)	nF	
Plasminelinoly	0-900000	800080 4E	FD	07 22	2 6B	78	6E	46	1B	07	1B	ØF	D9	10	13	40	N"	kxnF		e	
Elash size	0102 / D	800090 06	30	90 40	28	78	72	54	69	46	22	ดด	Ø1	FØ	69	F9	: 0	(vrT	iF"	i	
F 10511 5120	0132 ND	000070 00					~	40	~	40		40							~ ~		
		8000H0 BD	46	LS RI	10	82	90	40	96	48	AC.	42	00	D3	10	RD	· F · · ·	· · · · r	. K. B.		
		8000B0 62	68	20 68	3 00	21	D9	F6	32	FD	08	34	F4	E7	CØ	46	bh h		24	F	
		800000 04	94	12 00	9 ØC	94	12	00	70	B5	Ø5	00	07	48	ØE	ØØ			n	н	
		900000 14	00	00 F	. 122	ES	Q1	20	32	99	20	99	40	42	00	EØ			2 3 6	ap	
		000000 11	00	00 10		1.0	01	20	36	00	~ ~	00	-10	-14	00	10			····	· D	
		8000E0 11	F9	00 11	3 43	42	58	41	СЮ	B 2	20	BD	B5	10	C1	64		CBX8	p.		
		8000F0 80	21	FØ B5	5 3F	4B	40	4C	1B	69	85	BØ	22	00	18	00		SKGT	.i'	·	
		800100 49	ØØ	A A 93	3 Ø1	FØ	84	F8	3C	4 B	3D	4D	22	68	2B	60	I		<k=m'< td=""><td>'h+`</td><td></td></k=m'<>	'h+`	
		000110 20	40	00 4	40	Di	20	40	20	40	20	6	00	0.0	60	60	2W D	T /1			
		800110 30	40	78 44	\$ 40	DI	30	40	30	40	20	66	99	7.0	62	60	\N.D	L.//	NHT .	. . bn	+
		000120 01	20	10 10		77	na	DD	88	20	EE	na	074	22	20	AD	L.			1101	_
LOG	1 (22) 1																		-	•	8
- FFUnit: 4 co - CoreSight co - ROMTb1[0] @	de (BF) slots and U lit mponents: EOOFFOOO	eral slots																			^
- ROMTL1[0][0] - ROMTL1[0][1]	: E000E000, CID: B105E0 : E0001000, CID: B105E0	DD, PID: OOOBBOO8 S DD, PID: OOOBBOOA D	CS WT																		
- Rumibiluj[2] - Executing in	: E0002000, CID: B105E0 it sequence	JD, FID: OUUBBOOB F	гb																		
- Target inter	face speed: 4000 kHz (F	ixed)																			
- J-Link found	1 JTAG device. Core ID	0x0BC11477 (None)																			
- Connected su	ccessfully																				
<																					> .a
			_	_	_	_	_	_	-	_	_	_		_		_	_			_	_
rase, program a	and verify target									C	onne	ected	1	Cor	e Id:	0x0	BC114	77 5	peed:	4000	kH j



- (2) Option 2: Download by Keil
 - A. Copy [APOLLO_00_1V8.FLM] and [APOLLO_00_3V3.FLM] of BlueX file to the path under Keil_v5/ARM/Flash as below.

	Windows (C:) > Keil_v5 > A	ARM → Flash →			
	へ 名称	修改日期	类型	大小	
	 M29W640F	2020/5/29 16:36	文件夹		
7	RC28F640J3x_x2	2020/5/29 16:36	文件夹		
R	S29GL064Nx2	2020/5/29 16:36	文件夹		
*	SP29JL032H	2020/5/29 16:36	文件夹		
*	AM29F160DB.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29F160DT.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29F320DB.FLX	2015/7/8 16:30	FLX 文件	14 KB	
0529	AM29F320DBx2.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29F320DT.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29F320DTx2.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29x033.FLX	2015/7/8 16:30	FLX 文件	13 KB	
	AM29x128.FLM	2015/7/8 16:30	FLM 文件	13 KB	
	AM29x128.FLX	2015/7/8 16:30	FLX 文件	13 KB	
	AM29x800BB.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29x800BBx2.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29x800BT.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29x800BTx2.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29x800DB.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	AM29x800DBx2.FLX	2015/7/8 16:30	FLX 文件	14 KB	
	APOLLO_00_1V8.FLM	2019/9/27 8:59	FLM 文件	90 KB	
(C)	APOLLO_00_3V3.FLM	2019/9/27 8:59	FLM 文件	90 KB	

B. Follow the steps indicated in red arrow as below.

File Edit View Project Flash Debug	Peripherals Tools SVCS Window Help
- C 者 🖓 🖉 🕹 🖻	← → 作 陰 陰 健 揮 /// /// /// //// //////////////
🛞 🍱 🎬 🥔 🖼 🙀 template	
Project 4 X	by cdk3 code
Project: ble_base	
🖃 🔛 template	2
🗈 🪞 bx/core	3 * @file : .h 1
🗈 🦢 bx/ble	4 * gversion: 2
🖨 🦢 bx/log	6 * Shrief :
nr_micro_shell.c	7 🔣 Options for Target 'template' X **
ansi_port.c	
🕀 📄 ansi.c	9 Jevice Target Uutput Listing User U/U++ Asm Linker Jebug Utilities
	11 C Use Simulator <u>with restrictions</u> Settings C Use Simulator
bxsh_uart.c	12 Limit Speed to Real-Time
⊕ 🛄 bx_dbg.c	13 14 V Load Application at Statum V Bunto main() V Load Application at Statum V Bunto main()
B SEGGER_RTT.c	15 Initialization File
SEGGER_RTT_printf.c	16 Fr@ 5
bx_dbg_asm.s	
bx/drivers	19 Pestore Debug Session Settings Pestore Debug Session Settings
components	20 V Breakpoints V Toolbox V Breakpoints V Toolbox
bx_fifo.c	21 D Watch Windows & Performance Analyzer
user/profiles	22 I V Memory Display V System Viewer
user/service	24 - CPUIDU Parameter Driver DU Parameter
user_service_ble.c	25 SARMCM3.DLL SARMCM3.DLL */
user/app	26 Pides Pills Parameter Pides Pills Parameter
user_app.c	27 Dady DLL Frainleen. Dady DLL Frainleen. [7
user_ble.c	
user_ble_task.c	30
	31 Manage Component Viewer Description Files
E Ca	33 🖯
bx config.h	34 OK Cancel Defaultz Help
bx sys config.h	35
4	37 #ifndef HW_ECC_PRESENT
In Project	



C. In the pop-up, choose [Flash Download].

Cortex JLink/JTrace Target Driver Setup			×
Debug Trace Flash Download			
J-Link / J-Trace Adapter	SW Device		
SN:	IDCODE	Device Name	Move
	SWDI 🤆	ARM CoreSight SW-DP	Un
HW · V9.50 dll · V6.44f			
FW - U-Link V9 compiled Dec 13.2			Down
Port: Max	Automatic Detecti	on ID CODE:	
SW 🔻 5 MHz 💌	C Manual Configura	tion Device Name:	
Auto Clk	Add Delete	Undate IR len:	
Auto Cik	Delete	opulle	
Connect & Reset Options Connect: Normal Reset: Nor Reset: Nor Reset: Nor	rmal 💌	Cache Options ✓ Cache <u>C</u> ode ✓ Cache <u>M</u> emory ✓ Download Op ✓ Uerify Cod ✓ Download Op	tions e Download to <u>F</u> lash
CUSB C TCP/IP	ettings Po	ort (Auto: Autodetect	isc JLink Info
Scan 127 . (0.0.1:	0 Ring	Hink Cmd
State: ready	,	Fing	Junk end
		确定取消	应用(A)

D. Follow the steps as below. Choose [Apollo_00_3V3] when using RF01/RF03/RF04/BX2416/BX2417/BX2418 Module, or [Apollo_00_1V8] when using RF08.

Download Function Image: Constraint of the second seco	Trace Flash Do	vnload	
Programming Algorithm Description Device Size Device Type Address Range APOLLO_00_1V8 8M Ext. Flash SPI 00800000H - 00FFFFFFH RF08 choose APOLLO_00_1v8 RF01/RF03/RF04/BX2416/BX2417/2418 choose APOLLO_00_3v Start: 0x00800000 Size: 0x00800000 Add Remove	nload Function C Erase F Erase S C Do not	ull Chip	
Address Range APOLLO_00_1V8 RF08 choose APOLLO_00_1v8 RF01/RF03/RF04/BX2416/BX2417/2418 choose APOLLO_00_3v Start: 0x00800000 Size: 0x00800000 Add Remove	aramming Algorith		
RF08 choose APOLLO_00_1v8 RF01/RF03/RF04/BX2416/BX2417/2418 choose APOLLO_00_3v Start: 0x00800000 size: 0x00800000	escription	Device Size Device Type Address Range	
Add Remove	RF01/RF03/	RF04/BX2416/BX2417/2418 choose APOLLO_00_3v	3
	RF01/RF03/	RF04/BX2416/BX2417/2418 choose APOLLO_00_3v Start: 0x00800000 Size: 0x00800000	3
	RF01/RF03/	Add Remove	3
	RF01/RF03/	Add Remove	3
	RF01/RF03/	Add Remove	3
	RF01/RF03/	Add Remove	3

E. Before using this option, first, download bootloader of hex file by using J-Flash, e.g. [template_with_bootloader.hex] from SDK 3.x programming.



F. When connected to EVK by J-Link, procedures can be downloaded to EVK by the [Load] button indicated in red arrow as below.





4.2 Erase Flash Procedure

(1) The same process as procedure programming. After connected to EVK by J-Flash, follow the stpes as below, or press [F4], to erase Flash.

Eile Edit View	sh V6.44f - [new project	t*] indow Help						- 0	×
Name Host connection	Connect Disconnect		續料\软件 00	相关\SDK\BX	(Micro-SDK)	3-release-v3.2-2	20210104\SDK3\exa	mple 🗆 🗖 🗾	2
Taget interface Imit SWD speed SWD speed MCU Core Endian Check core ID Use target RAM Flash memory Base address Flash size	Production Program BlueX Apollo_00_1V8 CortexM0 Little No 132 KB @ 0x100000 8192 KB	ramming F7 ming F7 800030 DB 800040 07 800050 DB 800050 F8 800070 DB 800080 4E 800070 DB 800080 4E 800090 62 800080 62 800080 62 800080 64 8008080 64 8008080080 8008080080080 800080080 8008080080	1 2 3 8 32 3 Secur Unse Check Erase Progr Progr Verify Read Start 21 FØ B 00 00 9	4 5 4 00 80 1 e Chip cure Chip k Blank Sectors Chip ram aram & Verify back Application 5 3F 4B 6 8 01 F0 8	6 7 8 2 00 1C F2 F3 F4 F5 F6 F8 F9 40 4C 1B F8 3C	9 A B 14 60 00 1 00 3B 60 3 06 92 0F 1 46 60 78 6 07 1B 0F 1 1E 98 41 0 66 42 07 18 06 04 07 18 07 1B 0F 1 46 22 00 4 48 9C 20 08 4B 9C 42 09 90 02 20 00 42 29 00 4 92 70 00 10 69 85 10 10 48 30 40 2	C D E F AS 19 82 12 00 BX 11 01 29 31 10 08 31 10 08 31 10 08 31 10 08 32 10 08 33 10 08 33 10 10 08 33 10 13 40 N. 36 46 09 F6 39 10 13 40 N. 30 03 10 10 10 10 40 67 69 F9 10 10 10 41 47 48 0E 00 10 10 10 42 09 F0 12	CII 24; `5) iFBx .F. iF.x kxIFe .F. eC. A jFDx .F. ''. thF 'kxnFe .e(xrIiF''i 	1
2048 * 4 KB (- 2048 * 4 KB (- Start of prepa - End of prepa - Start of det - End of detain - CPU speed cor - Start of erasi - End of erasi - End of restor - Erase operati	2 0x00800000 wring flash programming ing flash programming mining dirty areas ild not be measured. ing chip ug chip oring on completed successful	flash cache	er 1.109 se	ייש שט איי ריש שט איי ניש					

(2) When erase completed, it will be as below.

SEGGER J-Fla File Edit View	ash V6.44f - [new proj v Target Options	ect *] Window Help	- 🗆 X
Project - ne	w p 🗖 🗖 🔀	E\BULEX\2_文档资料\软件相关\SDK\BXMicro-SDK3-release-v3.2-20210104\SE	K3\example 🗖 🔳 🔀
Name	Value	Address: 0x800000 x1 x2 x4	
Host connection	USB [Device 0]		E ACOLL
Target interface	SWD	Haaress 0 1 2 3 4 5 5 7 8 9 H B C D E	F HSCII -
Init SWD speed	4000 kHz	800000 42 58 32 34 00 80 12 00 16 14 00 00 19 82 12	00 BX24
SWD speed	4000 kHz	800010 00 00 04 00 00 07 00 08 00 3B 60 35 11 01	29; 5)
		800020 B0 B5 69 46 42 78 00 AF 92 06 92 0F D3 1D DB	08iFB×
MCU	BlueX Apollo_00_1V8	800030 DB 00 CB 1A 9D 46 05 00 69 46 00 78 01 F0 8E	F9FiF.×
Core	Cortex-M0	800040 07 21 01 20 6B 78 6C 46 1B 07 1B 0F DA 10 0B	40 kx1F0
Endian	Little	800050 98 40 A2 5C BD 46 10 40 43 1F 98 41 C0 B2 B0	BD P N F PC A
Lineck core ID	192 KR @ 0v100000	900060 F9 PE 60 46 44 79 00 0E 04 06 04 0E E2 10 DB	09 iEby
Use target hAM	132 KB @ 0x100000		
Flash memory	Internal bank 0	800070 JB 00 J3 1H YJ 46 05 00 22 00 00 21 68 46 JY	r6
Base address	0x800000	J-Flash V6.44f X 13	40 N"kxnF0
Flash size	8192 KB	69	F9 .:.@ <xrtif"i.< td=""></xrtif"i.<>
		10	BD .FL.K.B
		Frace experision completed successfully Completed after 1 051 sec. C0	46 bh h
		Prase operation completed successiony Completed after 1.031 sec	ØØН.
		00	FØ 2) ØB
		01	P4 CDVA
			04GBAHp
		确定 18	00
		28	60 IK=M"h+`
		800110 3C 4B 9A 42 4C D1 3C 4B 3C 48 2B 60 00 9B 62	68 <k.bl.<k<h+`bh< td=""></k.bl.<k<h+`bh<>
		000190 A1 CO 10 10 TT TT AT TT AR TO AR 90 ET NA 00 99 90	AD L 74 000
LOG			
- 2048 * 4 KB	@ 0v00800000		
- Start of pre	paring flash programm	ng	^
- End of prepa	ring flash programmin		
- Start of deter	ermining dirty areas : mining dirty areas	n Ilash cache	
- CPU speed co	uld not be measured.		
- Start of era	sing chip		
- Ind of erasi: - Start of res	ng chip toring		
- End of resto	ring		
- Erase operat	ion completed success	ully - Completed after 1.051 sec	¥
<			>



4.3 Degug and Check the Log

- (1) Debug by Keil
 - A. In Keil, click [Start Debug], and make sure J-Link is well-connected during debugging.

ExBXMicro-SDK3-release-v3.2-20210104/SDK3/examples/ble/ble_base/project/mdk/ble_base.uvprojx - µVision Start/Stop debug	- 0	×
Ele Edit View Broject Figsh Debug Perjohensis Iools SVCS Window Help		
🗈 📴 🚂 🖉 🗼 🖦 🚓 🛛 Single step-debugging 🗷 //// 🕼 🕫 🕫 18,76,492,33M,0CC 🖳 象 🙋 🔍 📀 🔗 🎪 💽 🐁		
Registers 🔪 🗣 🖬 Disassembly		a 🗵
Register Vilue 0000000355 7D20 LDRB r0,[r4,40x14]		^
1 0x0000 0x0000035E 68E1 LDR r1,[r4,≢0x0C]		~
		>
H CHOILE buyys, configh buysic], ortigh		▼ ×
- 80 00002 135 //#define RF_TX_FOWER_2DBM_DCDC_OFF_3V3 0x2		^
12 01777 136 //fdefine RF TX FOWER 200M DCDC OFF 1V8 0x3		
B 04777 133 //define RF IX PORE NOBR DCDC ON 0X5		
110 07777 139 //#define RF_TX_POWER_4DBM_DCDC_OFF_3V3 0x6		
140 //#define RF_TX_FOWER_80BM_DCDC_OFF_3V3 0x7		
113 (ST) 040012. 141 //#define RF_TX_FOWER_8DBM_DCDC_ON_3V3 0x8		
C-1258 9ad100 144 EFInder RF_TX_POWER		l l
System Ids forfine RF_TX_POWER Ox5		
B-Intenal 199 Penair		
149 estinder BX_DEV_NAME		
150 #define BX DEV NAME "BLUEX-SDR3"		
Register 153 B #ifndef BX_MAC_ADDR		
154 #define BX_MAC_ADDR {0xee,0x55,0x66,0x77,0x88,0x99}		
155 Fendir 156		~
Project Registers C		>
Command P 🔲 Call Stack + Locals		4 🖬
^ Name Location/V Type		
John -si\Dahlacto-puts-reiteservs.a=autour\Johns\Texamples\Late\Late\Late\Late\Late\Late\Late\Late		
* JLink Info: Reset: Reset device via AIRCR.SYSRESEIREQ.		
BS \/template\///components/ble/controller/driver/flash_cache.c\l36, 1		
ss \\template\///components/bluex/ble/controller/driver/riasn_cache.c\143, 1		
c >		
2		
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakAccess COVERAGE DEFINE DIR 🚱 Call Stack + locals 🗐 Memory 1		
J-UNK/J-TRACE Cortex t1: 0.0000000 sec L151 C/7	CAP NUM SCRL O	VR R/W

- (2) Check Log by RTT Viewer
 - A. To output Log print, IC should be programmed with log-enabled firmware first.
 - B. In SDK 3.x, there're 2 macro definitions in [bx_sys_config.h] to setup Log. Follow the steps as below to activate RTT Log.

<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>P</u> roject Fl <u>a</u> sh <u>D</u> ebug	Peripherals Tools SVCS Window Help	
n 📬 🛃 🖉 🐰 🛍 📸 🔊 🕲	🖛 🔿 🕐 陰 陰 🚷 🛱 譚 🎼 /版 🖄 advData 🛛 🔽 🗟 🥔	🍳 🔺 🔹 🔗 🏤 🖬 📲
🗇 🍱 🕮 🥔 🔛 🙀 template	🔍 🔊 📥 🖶 🗇 🐡 🎰	
Project 📮 🗵	bx_sdk3_config.h bx_ip_config.h bx_config.h bx_sys_config.h	Clk_gate.c arch_init.c bx_app_config.h
😐 🗋 ansi_port.c 🔺	46 #define CFG ON CHIP	1
	47 #endif	
	48 -	
n bysh uart c	49 🖂 #ifndef CFG_SYS_LOG	
by dbg c	50 #define CFG_SYS_LOG	1
	51 #endif	
SEGGER_RTLC	53 Hifndef CEG DYNAMIC UPDATE	
B SEGGER_RTT_printf.c	54 #define CFG DYNAMIC UPDATE	1
bx_dbg_asm.s	55 #endif	
bx/drivers	56 -	
😑 🦢 components	57 = #ifndef ENABLE_CANNEL_CONN_PARA_UPD_FEATURE_PATCH	
⊞- 🗋 bx_fifo.c	58 #define ENABLE_CANNEL_CONN_PARA_UPD_FEATURE_PATCH	0
🗄 🚞 user/profiles	59 #endif	
🖃 🦢 user/service	61 Sifndef ENABLE LLC CON HDD DEO IND HANDLED DATCH	
user service ble.c	62 #define ENABLE LLC CON UPD REQ IND HANDLER FATCH	0
user/ann	63 #endif	
	64 -	
user_app.c	65 = #ifndef ENABLE_ADV_PAYLOD_31BYTE_PATCH	
user_ble.c	66 #define ENABLE_ADV_PAYLOD_31BYTE_PATCH	0
	67 #endif	
⊕ user_ble_profile.c	60	
- 🗁 user/drivers	70 #define PATCH SKIP H4TL READ START	0
🖨 🦾 cfg	71 #endif	
bx_config.h	72 -	
bx_sys_config.h	73 = #ifndef TX_TEST_PACKET_NUM_PATCH	
bx pcb config.h	74 #define TX_TEST_PACKET_NUM_PATCH	1
by app config b	75 #endif	
by in configh	70 - 77 Difindef MESH SCHED DATCH	
D by all 2 and 5 b	78 #define MESH_SCHED_PATCH	0
DX_SGK3_CONTIG.N	79 #endif	
	80 -	
	81 sifndef BX_VERF	
	82 #define BX_VERF	0
	83 #endif	
	85 Diifndef VRAT MILLIVOLT	
	86 #define VBAT MILLIVOLT	4200
4 7 7		



C. BlueX chips cannot connect J-Link during sleep mode. Developers can define [DEBUGGER_ATTACHED] of [bx_sys_config.h] as [1] as reference below. When [DEBUGGER_ATTACHED] defined as 1, chips can connect J-Link during sleep mode, which is easy for debugging. To reduce power consumption during sleep mode, please define [DEBUGGER_ATTACHED] as [0] after debugging.

<u>File Edit View Project Flash Debug</u>	Petjpherals Iools SVCS Window Help
🗎 💕 🖬 🖉 🐰 🖦 🏝 🤊 🕾	← ⇔ 箆 毘 段 芘 诓 //: //: //: //: //: //: //: //: //: /
🗇 🔝 🕮 🥔 🧱 🙀 template	🛛 🔊 着 着 🔶 💩
Project 🔉 🛙	bx_sdk3_config.h bx_jbc_config.h bx_config.h bx_config.h bx_sor_config.h ck_gate.e arch_init.e bx_app_config.h bx_bx_config.h user_app.c user_service_ble.c
🖃 🍄 Project: ble_base 🔺	167 #endif
😑 💭 template	168
🐵 🧰 bx/core	169 Stifner EXT WARE UP ENABLE
🐵 🧰 bx/ble	170 statine EAT WARD_OF_ENABLE 1 171 iendif
🖨 🦢 bx/log	172 -
Inr_micro_shell.c	173 ====================================
ansi_port.c	174 Hindef LPCLK DRIFT MAX
ansi.c	1/3 FORTING LIVER DATE THAN 20
bx_shell.c	177 felse
bxsh_uart.c	178 #define LPCLK_DRIFT_MAX 500
bx_dbg.c	179 #endif
B SEGGER_RTT.c	190 (Assessment Debug second #/
SEGGER_RTT_printf.c	102 #ifndef DEBUGGER ATTACHED
bx_dbg_asm.s	183 #define DEBUGGER ATTACHED 1
🗉 🧰 bx/drivers	184 #endif
🖃 🦢 components	
bx_fifo.c	180 // guille bo not makebr
🖲 🦢 user/profiles	188 Difindef FREERTOS_WAKEUP_DELAY
user/service	189 #define FREERTOS_WAKEUP_DELAY (BLE_WAKEUP_TIME - 200)
user_service_ble.c	190 #endif
😑 🦢 user/app	191 192 #ifndef XTAL STARTUP TIME
user app.c	193 #define XTAL STARTUP TIME 10
. user ble.c	194 #endif
. user_ble_task.c	
	197 Heffine LDO 3VI OUTPUT SIERF RET
user/drivers	198 #endif
😑 🦢 cfg	199 -
bx_config.h	200 #ifndef LDO LVS OUTPUT SLEEP RET
bx_sys_config.h	201 Facture LDG_VS_OUTPUT_SLEEP_KET
bx pcb config.h	203 -
bx app config.h	204 d#ifndef VDD_1V8_SLEEP_LDO1
bx ip config.h	205 fdefine VDD_1V8_SLEEP_LDO1 1
hu adh2 ganfia h	200 Fenair 207 -
	200
🔚 Project 🌍 Books 🛛 {} Func 🛛 🕁 Temp	C

- D. After adjustment above, use Keil to compile and program firmware to EVK, then use RTT Viewer to check the Log.
- E. Check RTT Viewer.



F. In configuration, we need to setup [Specify Target Device] by choosing [APOLLO_00_1V8] or [APOLLO_00_3V3]. Next, choose [SWD] and [4000kHz] in Target Interface& Speed. Then, choose [Auto Detection] in RTT Control Block. When finished, click [OK] to check RTT Log.

J-Link RTT Viewer V6.46j	
Terminals Input Logging Help	
All Terminals Terminal 0	
J-Link RTT Viewer V6.46j Configuration	7 ×
Connection to J-Link	
● USB □ Serial No	
○ ICP/IP	
O Existing Session	
Specify Target Device	
APOLLO_00_1V8	··· ·
Script file (optional)	-
Target Interface & Speed	
SWD	• 4000 kHz •
RTT Control Block	
Auto Detection O Address O	Search <u>R</u> ange
J-Link automatically detects the RTT cont	trol block.
OK	Cancel



G. RTT Log as below.

🔜 J-Link RTT Viewer V6.46j				
<u>File</u> <u>Terminals</u> Input Logging <u>H</u> elp				
Log All Terminals Terminal 0				
00> rc_calib loop count i=4436				
00> rc_calib loop count i=6621				
00> rc_calib loop count i=6705				
00> rc_calib loop count i=6743				
00> rc_calib loop count i=6766				
00> rc_calib loop count i=6696				
00> rc_calib loop count i=6798				
00> rc_calib loop count i=6803				
00> rc_calib loop count i=6714				
00> I/ARCH INIT:main				
00> RO=0x2A				
<pre>00> I/osapp.utils:osapp_utils_set_dev_init,role=0xA</pre>				
00> bond_manage_init				
00> uart framing error				
00> W/osapp.uart_server:gapm_cmp_evt operation:0x1				
00> soft wakeup				
00> I/osapp.uart_server:noti status:67				
00> soft wakeup				



5. Revison History

Version	Description	Date (YYYY/MM/DD)	Author
1.0	Initial version	2020/02/04	姚琪
1.1	Added content of ENK	2020/02/05	淡明洁
1.2	Amended content of debug	2020/03/03	夏杰
1.3	Amended content of EVK and cover, added index	2020/07/17	简任锋
1.4	Updated content of EVK, added appendix	2021/01/18	简任锋
1.5	Amended Chapter4 and updated pictures	2021/06/11	简任锋
1.6	English version update	2021/06/16	Michelle
1.7	Added BX2400-eRF01e-G1a diagram and EVK introduction	2021/08/11	简任锋

6. Appendix

6.1 Schematic of BX2400-dRF0xp-S1c



6.2 Schematic of BX2400-eRF01e-G10



6.3 Schematic of BX2400-eRF01e-G1

